First IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

3D-TEST

in conjunction with ITC / Test Week 2010
Convention Center - Austin, Texas, USA
November 4+5, 2010
http://3dtest.tttc-events.org

Call for Participation

The new 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs). While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Workshop Program – The workshop program contains the following elements.

- Keynote address: "Testing In a New Dimension"
  by Bob Patti, CTO of Tezzaron Semiconductor, USA
- Invited Address: "An Integrated Approach to Design and Test of 3D ICs"
  by Brion Keller, Senior Architect, Cadence Design Systems, USA
- Various paper and invited presentation sessions
- Continuous poster display and Table-Top Demos
- A panel session

For the detailed version of the program, please turn over.

Participation – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes all technical sessions, Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as far as made available by their presenters), workshop reception, continental breakfast, lunch, and break refreshments. On-line registration is available via the workshop's website (http://3dtest.tttc-events.org). Alternatively, register on-site during Test Week at the ITC Registration Counter at the Austin Convention Center; admission for on-site registrants is subject to availability.

Further Information

Yervant Zorian – *General Chair*
Synopsys Inc.
47100 Bayside Parkway
Fremont, CA 94538, USA
Tel.: +1 (510) 360-8035
Fax: +1 (510) 360-8078
E-mail: yervant.zorian@synopsy.com

Erik Jan Marinissen – *Program Chair*
IMEC vzw
Kapeldreef 75
B-3001 Leuven, Belgium
Tel.: +32 (0)16 28-8755
Fax: +32 (0)16 28-1515
E-mail: erik.jan.marinissen@imec.be

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Workshop Program

Thursday November 4, 2010

Session 1: Opening

Moderator: Mike Ricchetti – AMD, USA

16:00h: **Welcome Address**
General Chair: Yervant Zorian – Synopsys, USA
Program Chair: Erik Jan Marinissen – IMEC, B

16:15h: **Keynote Address**:
Testing in a New Dimension
Bob Patti – Tezzaron Semiconductor, USA

3D circuit integration offers a new level of system integration. The number of transistors on a chip can be doubled, quadrupled, or more; new process and function mixes, previously at the bleeding edge of possibility, can now become mainstream. The ability to mix technologies at the micron scale opens doors to system miniaturization and new architectures, an advance as revolutionary as the shift from transistors to integrated circuits. However, 3D also demands new testing techniques. It extends the continuing need to test and verify ever more transistors, but it also requires the testing of disparate component types such as integrated analog, sensors, DRAM, Flash, and power supplies, all in the same integrated circuit. Many functions may be hidden from typical test access connections, and some might not be readily testable in their normal modes of operation. New, innovative, compact testing schemes are called for and more robust methods for self test will be required. This presentation will examine current 3D efforts and the direction of 3D integration. It will also look at some of the methods currently being employed to improve testability, self test performance, and self-repair.

Session 2: 3D Design-for-Test

Moderator: Stephen Pateras – Mentor Graphics, USA

17:00h: **Invited Address**:
An Integrated Approach to Design and Test of 3D ICs
Brion Keller – Cadence Design Systems, US

As 3D stacking drives new design and integration methodologies, the manufacturing test aspects must be considered early on in the design phase to ensure high testability and predictability, both at the die/wafer tier level and final package testing. Among other things, this requires a framework to both model the complex interactions between design and test as well as enable quick trade-offs between different DfT architectures and partitioning decisions. This talk will outline the key integration challenges and innovative approaches to address these challenges with high predictability.

17:30h: Embedded Test Resource Partitioning for Memories in a 3D-IC Context
Yervant Zorian – Synopsys, USA

17:45h: Functional/Structural Test Boundaries for 3D-IC
Rob Aitken, Teresa McLaurin, Sachin Idgunji – ARM, USA

18:00h: Standardization for 3D-Testing
Erik Jan Marinissen – IMEC, B

18:15h: Mini-Panel

Session 3: Posters and Demos

18:30h: For list of Posters and Table-Top Demos: see next page.

Workshop Reception

19:00-21:00h

Friday November 5, 2010

Workshop Breakfast

07:00-08:00h

Session 4: Pre- and Post-Bond Testing

Moderator: Tapan Chakraborty – Alcatel-Lucent, USA

08:00h: KGD Probing of TSVs at 40um Array Pitch
Ken Smith, Peter Hanaway, Mike Jolley, Reed Gleason, Chris Fournier, Eric Strid – Cascade Microtech, USA

08:30h: Sharing of Logic and Test TSVs for Testing of 3DICs
Shravan Garlapati, Michael S. Hsiao, Leylay Nazhandali – Virginia Tech, USA

09:00h: Applying Electric Fault Simulation for Deriving Tests for TSVs
Matthias Gulbins, Fabian Hopsch, Peter Schneider, Bernd Straube, Wolfgang Vermeiren – Fraunhofer IIS/EAS, D

09:30h: Impact of Various Test Flows on the Cost in 3D D2W Stacking
Mottaqiallah Taouil, Said Hamdioui – Delft Univ. of Technology, NL; Erik Jan Marinissen – IMEC, B

Session 5: Posters and Demos

10:00h: For list of Posters and Table-Top Demos: see next page.
Coffee and tea provided.

Session 6: TSV Testing

Moderator: Craig Bullock – Texas Instruments, USA

10:30h: Comparing Through-Silicon Via Void/Pinhole Defect Self-Test Methods
Yi Lou, Zhuo Yan, Fan Zhang, Paul Franzon – North-Carolina State Univ., USA

11:00h: Multi-Scale Simulation and Characterization for Stress Management in 3D IC TSV-Based Integration Technology: Stress Assessment for Chip Performance
Valeriy Sukhavev, Armen Kteyan, Nikolay Khachatryan, Henrik Hovsepyan, Jun-Ho Choy – Mentor Graphics, USA; Ehrenfried Zschech, Rene Huebner – Fraunhofer IZFP, D

11:30h: Electrical Tests for Three-Dimensional ICs with TSVs
Hao Chen, Jian-Yu Shih, Shih-Wei Li, Hung-Chih Lin, Min-Jer Wang, Ching-Nen Peng – TSMC, TW

Workshop Luncheon

12:00-13:00h

Session 7: Posters and Demos

13:00h: For list of Posters and Table-Top Demos: see next page.

Session 8: 3D-SIC Applications and Test

Moderator: Samy Makar – Apple, USA

13:30h: 3D-TSV Technology: A DfT and Test Perspective
Michael Laisne, Rajamani Sethuram – Qualcomm, USA

13:45h: A Configurable Sheet of Wide I/O Memory for Stacking Under a Variety of High-Power ASICs
Peter M. O'Neill, Chinmay Gupte – Avago Technologies, USA

14:00h: Wide-IO 3D for Multimedia Application Processors: Operational Nightmares?
Stephane Lecomte – ST-Ericsson, USA

14:15h: From Stacked to 3D Devices
Vincent Chalendard, Olivier Alavoine, Adin Hyslop, Christophe Sucur, Jean-Pierre Gibaux – Texas Instruments, FR

Session 9: Panel Discussion

14:30h: **Challenges and Solutions in 3D Wafer Probing**

Moderator: Erik Jan Marinissen – IMEC, B

Panelists: Marc Loranger – FormFactor, USA
Wayne Moorhead – Scanimetrics, CAN
Jay Orbon – Verigy, USA
Dan Rishavy – TEL, USA
Ken Smith – Cascade Microtech, USA
Andy Yiin – Intel, USA

16:00h: Workshop Closure

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Posters and Table-Top Demos

Posters

Posters are on display throughout the workshop.
Dedicated poster sessions

- Thursday November 4: 18:30-19:00h
- Friday November 5: 10:00-10:30h and 13:00-13:30h

Poster 1: Power Constrained Test Scheduling for 3D Stacked Chips
Breeta SenGupta, Urban Ingelsson, Erik Larsson – Linköping University, SE

Poster 2: Parallel Test of Identical Cores Using Test Elevators in 3D Circuits
Alberto Bosio, Giorgio di Natale – LIRMM, FR

Poster 3: Interconnect Built-In Self-Repair and Adaptive Serialization (I-BIRAS) for 3D Integrated Systems
Michael Nicolaidis, Lorena Anghel, Vladimir Pasca – TIMA, FR

Poster 4: Die-Wrapper Optimization for 3D Stacked ICs
Brandon Noia, Krishnendu Chakrabarty – Duke University, USA; Erik Jan Marinissen – IMEC, B

Poster 5: A Standardizable 3D DfT Architecture
Erik Jan Marinissen – IMEC, B; Chun-Chuan Chi – Natl. Tsing-Hua University, TW; Jouke Verbree – Delft University of Technology, NL; Mario Konijnenburg – IMEC-NL, NL

Poster 6: 1149.3D?! – Leveraging Test Access Standards for 3D-SICs
Adam Ley, Alfred L. Crouch – ASSET-Intertech, USA

Poster 7: Design and Test of 3D-MAPS, a 3D Die-Stack Many-Core Processor
Dean L. Lewis, Michael B. Healy, Mohammad H. Hossain, Tzu-Wei Lin, Mohit Pathak, Hemant Sane, Sung Kyu Lim, Gabriel H. Loh, Hsien-Hsin S. Lee – Georgia Tech, USA

Poster 8: Wireless Wafer Test for Iterative Testing During System Assembly
Z. Noun – LIRMM, FR; Philippe Cauvet – OPHTIMALIA, FR; Marie-Lise Flottes, D. Andreu, Serge Bernard – LIRMM, FR

Poster 9: New Testing Technique for Copper TSV in 60GHz Wireless Applications
Sukeshwar Kannan, Bruce Kim – University of Alabama, USA

Poster 10: A Wafer Ordering Heuristic for Iterative Wafer Matching in W2W 3D-SICs with Diverse Die Yields
Eshan Singh – Stanford University, USA

Table-Top Demos

Table-top demos are on display throughout the workshop.
Dedicated demo sessions

- Thursday November 4: 18:30-19:00h
- Friday November 5: 10:00-10:30h and 13:00-13:30h

Demo 1: IEEE 1149.1-2011, Multi-TAP iMajik and Concurrent JTAG for 3D-SICs
CJ Clark – Intellitech, USA

Demo 2: Wireless Probe, Test and Interconnect Solutions for Multi Die Packages
Chris Sellathamby, Wayne Moorhead – Scanimetrics, CAN

Demo 3: Emulating 3-D Chip Stack in FPGAs with IJTAG Access to Test Structures
John Potter - ASSET InterTech, USA

Demo 4: New Publications from Springer of Interest to Attendees of 3D-TEST Workshop
Charles Glaser – Springer, USA

For more information: http://3dtest.tttc-events.org

Corporate Supporters

The 3D-TEST Workshop gratefully acknowledges the financial support from the following companies

ADVANTEST, ARM, Intellitech, Mentor Graphics, SCANIMETRICS, SYNOPSYS, SYNTEST, Tezzaron Semiconductor, TOKYO ELECTRON

IEEE, IEEE computer society, tttc, ITC International Test Conference