First IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

3D-TEST

in conjunction with ITC / Test Week 2010
Convention Center - Austin, Texas, USA
November 4+5, 2010
http://3dtest.tttc-events.org

General Chair:
Y. Zorian – Virage Logic (US)

Program Chair:
E.J. Marinissen – IMEC (B)

Finance Chair:
Said Hamdioui – TU Delft (NL)

Publication Chair:
M. Grosso – Politecnico di Torino (I)

Publicity Chair:
F. von Trapp – 3DInCites (US)

Web Chair:
G. Jervan – Tallinn Univ. of Techn. (EE)

Local Arrangements Chair:
J. Potter – Asset Intertech (US)

Program Committee Members:
S. Adham – TSMC (CAN)
V. Agrawal – Auburn Univ. (US)
S. Bhatia – Oasys (US)
C. Bullock – Texas Instruments (US)
K. Chakrabarty – Duke Univ. (US)
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T. Eaton – Cisco Systems (US)
G. Fleeman – Advantest (US)
M.-L. Flottes – LIRMM (F)
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M. Higgins – Analog Devices (IRL)
S.-Y. Huang – NTHU (TW)
R. Kapur – Synopsys (US)
M. Knox – IBM (US)
M. Laisne – Qualcomm (US)
P. Lebourg – ST Microelectronics (F)
S. Lecomte – ST-Ericsson (F)
H.-H. Lee – Georgia Tech (US)
D. Lefever – Advantest (US)
I. Loi – Universita di Bologna (I)
M. Loranger – FormFactor (US)
T. McLaurin – ARM (US)
N. Minas – IMEC (B)
W. Moorhead – Scanimetrics (CAN)
K. Parker – Agilent Technologies (US)
S. Pateras – Mentor Graphics (US)
B. Patti – Tezzaron Semiconductor (US)
F. Pöhl – Infineon Technologies (D)
M. Ricchetti – AMD (US)
D. Rishavy – TEL Test Systems (US)
T. Thärigen – Cascade Microtech (D)
E. Volkerink – Verigy (US)
L. Whetsel – Texas Instruments (US)
Y. Xie – Penn. State Univ. (US)
Q. Xu – Chinese Univ. Hong Kong (HK)

Table-Top Demos and Corporate Support

The new 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs). While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Table-Top Demos – The 3D-TEST Workshop offers the opportunity to present Table-Top Demos during the workshop. Table-Top Demo participants get a table and electricity outlet provided by the workshop. A Table-Top Demo presentation may include displaying slides or demoing tools. Typical content may be comprised of technical descriptions, case studies, best practices, and user testimonials of products or solutions. These presentations will be listed in the workshop program booklet along with the regular paper sessions, and should be targeted to the workshop's technical audience. Table-Top Demos differ from other workshop presentations in that a company name, logo, and product name may be mentioned explicitly. Proposal selection is based on technical content and relevance to 3D-TEST audience and topics. Table-Top Demo tables will be assigned in a first-come-first-served order, but priority will be given to Corporate Supporters (see below). If you are interested in presenting a Table-Top Demo, please contact the workshop's Program Chair Erik Jan Marinissen at <erik.jan.marinissen@imec.be.>

Corporate Support – Companies are invited to provide financial support to the 3D-TEST Workshop. In return, the supporting corporations will be recognized by the workshop in various ways, including: display corporate logo on workshop's website, program booklet, projection screen, Electronic Workshop Digest, etc. Corporate supporters get priority in the assignment of available Table-Top Demos. For additional details, please contact the workshop's Finance Chair Said Hamdioui at <s.hamdioui@tudelft.nl>.

Key Dates

- Submission deadline for posters : **October 15, 2010**
- Notification of acceptance : **October 18, 2010**
- Submission of Table-Top Demo proposals : **October 1, 2010**
- Camera-ready material : **October 22, 2010**

Further Information

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Call for Poster Submissions

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Topic Areas – You are invited to participate and submit your contributions to the 3D-TEST Workshop. The workshop's areas of interest include (but are not limited to) the following topics:

- *Defects due to Wafer Thinning*
- *Defects in Intra-Stack Interconnects*
- *DfT Architectures for 3D-SICs*
- *EDA Design-to-Test Flow for 3D-SICs*
- *Failure Analysis for 3D-SICs*
- *Known-Good Die / Stack Testing*
- *Pre-Bond and Post-Bond Testing*
- *Reliability of 3D-SICs*
- *Standardization for 3D Testing*
- *System/Board Test Issues for 3D-SICs*
- *Test Cost Modeling for 3D-SICs*
- *Test Flow Optimization for 3D-SICs*
- *Tester Architecture incl. ATE and BIST*
- *Thermal/Mechanical Stress in 3D-SICs*
- *TSV Test, Redundancy, and Repair*
- *Wafer Probing and Probe Damage of 3D-SICs*

Submission Instructions – Submission of papers in closed now. However, it is still possible to submit proposals for poster presentation. Submissions must be sent in as PDF file. The Workshop prefers Full Paper submissions (of up to six pages), but also allows (Extended) Abstract submissions. Detailed submission instructions can be found at the Workshop's website: http://3dtest.tttc-events.org. All submissions will be evaluated for selection with respect to their suitability for the workshop. Selected submissions can at this point only be accepted for poster presentation at the Workshop.

Publications – The workshop will make available to all participants an Electronic Workshop Digest, which includes all material that authors are willing to provide: abstract, paper, slides, poster, etc. Authors of a selected subset of submissions will be invited to submit extended journal versions of their manuscripts to be considered for a Special Issue of Springer's 'Journal of Electronic Testing – Theory and Applications' (JETTA) being planned for 2011.

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