The 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs). While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Workshop Program – The workshop program contains the following elements.

- **Keynote address:** “3-D SoC Packaging for Smart Mobile Devices: Current State and Challenges” by Hong Hao, VP Media SoC Development, Samsung Semiconductor, Inc.
- **Invited Address:** “3D TSV Infrastructure: Challenges and Opportunities” by E. Jan Vardaman, President, TechSearch International, Inc.
- Five sessions with in total 17 paper presentations.
- Continuous display of posters and table-top demos.
- Two panel sessions: one with industry executives on 3D-Test, and one on (Wide-I/O) DRAM stacking.

For the detailed version of the program, please turn over.

**Call for Participation**

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**Participation** – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes all technical sessions, Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as far as made available by their presenters), workshop reception, continental breakfast, lunch, and break refreshments. On-line registration is available via the workshop’s website (http://3dtest.tttc-events.org). Alternatively, register on-site during Test Week at the ITC Registration Counter at the Disneyland Hotel; admission for on-site registrants is subject to availability.

Further Information

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Second IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

in conjunction with ITC / Test Week 2011
Disneyland Hotel - Anaheim, California, USA
September 22+23, 2011
http://3dtest.tttc-events.org

Workshop Program

Thursday September 22, 2011

Session 1: Opening
Moderator: Peter Maxwell – Aptina Imaging, USA
16:00h: Welcome Address
  General Chair: Yervant Zorian – Synopsys, USA
  Program Chair: Erik Jan Marinissen – IMEC, B

16:15h: Keynote Address:
  3-D SoC Packaging for Smart Mobile Devices: Current State and Challenges
  Hong Hao – Samsung Semiconductor, USA

17:00h: Invited Address:
  3D TSV Infrastructure: Challenges and Opportunities
  E. Jan Vardaman – TechSearch International, USA

Session 2: Panel Discussion
17:30h: Executive Views on 3D-Test Challenges and Solutions
Moderator: Yervant Zorian – Synopsys, USA
Co-organized with Herb Reiter, GSA / 3D-IC Working Group
Panelists: Hong Hao – Samsung Semiconductor, USA
  Ken Lanier – Teradyne, USA
  Eric Strid – Cascade Microtech, USA
  Sargis Taneja – Cadence Design Systems, USA

Session 3: Posters and Demos
18:30h: For list of Posters and Table-Top Demos: see next page.

Workshop Reception
19:00-21:00h

Friday September 23, 2011

Workshop Breakfast
07:00-08:00h

Session 4: Research
Moderator: Sudipta Bhawmik – Qualcomm, USA
08:00h: Thermal-Aware Test Scheduling for 3D ICs
  Chih-Yao Hsu, Chun-Yi Kao, James C.-M. Li – National Taiwan University, TW;
  Krishnendu Chakrabarty – Duke University, USA

08:15h: Variable Output Thresholding: A Robust Delay Measurement Scheme for TSV
  Shi-Yu Huang, Yu-Hsiang – National Tsing Hua University, TW; Ding-Ming Kawai – IFUT, TW

08:30h: Test Planning for 3D Stacked ICs with Through-Silicon Vias
  Brea SenGupta, Urban Ingelsson, Erik Larsson – Linköping University, SE

08:45h: Pre-Bond Testing of Die Logic and TSVs in High Performance 3D-SICs
  Brandon Noia, Krishnendu Chakrabarty – Duke University, USA

Session 5: Electronic Design Automation
Moderator: Saman Adham – TSMC, Canada
09:00h: Automation of 3D DIT Insertion
  Sergei Deutsch – Cadence, DE; Vivek Chickermmane, Brion Keller – Cadence, USA;
  Subhasish Mukherjee – Cadence, IN; Mario Konijnenburg – IMEC/Holst Centre, NL;
  Erik Jan Marinissen – IMEC, BE; Sandeep K. Goel – TSMC, USA

09:15h: DIT and Test Flows for Stacked Die
  Etienne Racine, David Buck, Steve Pateras – Mentor Graphics, USA

09:30h: 3D Design, Test Technology, and Standardization
  Adam Cron – Synopsys, USA

09:45h: Architectures for Testing 3D Chips Using Time-Division Demultiplexing/Multiplexing
  Laun-Terrng Wang, Shianling Wu, Marish Bhattarai, Fangfang Li, Zhigang Jiang – SynTest Technologies, USA;
  Nur A. Toub – University of Texas, USA; Michael S. Hsiao – Virginia Tech, USA;
  Jian-Liang Huang, James Chien-Mo Li – National Taiwan University, TW; Xiaoqing Wen – Kyushu Institute of Technology, JP

Session 6: Posters and Demos
10:00h: For list of Posters and Table-Top Demos: see next page.

Coffee and tea provided.

Session 7: Wafer Probing
Moderator: Amy Leong – MicroProbe, USA
10:45h: Probing Strategies for Through-Silicon Stacking
  Eric Strid, Ken Smith, Peter Hanaway, Reed Gleson – Cascade Microtech, USA

11:00h: Challenges and Solutions for Testing of TSV and Micro-Bump
  Ben Eldridge, Marc Loranger – FormFactor, USA

11:15h: A Low-Force MEMS Probe Solution for Fine-Pitch 3D-SIC Wafer Test
  Matt Losey, Robert Smith, Flored Cros, Yohannes Desta, Lakshmi Namburi, Melvin Khoo – Touchdown Technologies, USA

Session 8: Standardization
Moderator: Dan Hamling – GE Capital, USA
11:30h: Standards for 3D Stacked Integrated Circuits
  Richard A. Allen – NIST, USA; Larry Smith – Sematech, USA

11:45h: Status Update of IEEE P1838
  Erik Jan Marinissen – IMEC, BE; Adam Cron – Synopsys, USA

Workshop Luncheon
12:00-13:00h

Session 9: Posters and Demos
13:00h: For list of Posters and Table-Top Demos: see next page.

Session 10: Applications
Moderator: Dan Rishavy – TEL Test Systems, USA
13:30h: Product Level Screening of Latent Defects in Through Silicon Vias
  Cathal Cassidy, Simon Watts, J. Couper, J. Terau, M. Steiner, P. Dorfi, J. Kraft, F. Schrank – Austria Microsystems, A;
  E. Bottino – NXP Semiconductors, A

13:45h: Test Challenges in 3D TSV SOC
  Amer Cassier – Qualcomm, USA

14:00h: Electro-Migration Behavior of 3DIC TSV – Comparison of Usual Thin Metal Line vs. Thick Metal Line Process
  Thomas Frank, C. Chappaz, L. Arnaud, F. Lorut – STMicroelectronics, FR;
  S. Moreau, P. Leduc, A. Thuaire – CEA-LETI, FR; Lorena Anghel – TIMA, FR

14:15h: Realize Dynamic Testing Based on Thermal Perspective
  Chen Hao, Min-Jer Wang, Hung-Chih Lin, Ching-Nen Peng – TSMC, TW

Session 11: Panel Discussion
14:30h: Test Challenges and Solutions for (Wide-I/O) DRAM Stacking
Moderator: Bill Eklow – Cisco Systems, USA
Panelists: Gary Freeman – Advantest, USA;
  Sandeep K. Goel – TSMC, USA;
  Marc Greenberg – Cadence Design Systems, USA;
  Michael Laisne – Qualcomm, USA;
  Mike Ricchetti – AMD, USA

16:00h: Workshop Closure
Posters and Table-Top Demos

Posters

Posters are on display throughout the workshop.

Dedicated poster sessions
- Thursday September 22: 18:30-19:00h
- Friday September 23: 10:00-10:45h and 13:00-13:30h

Poster 1: Test Cost Modeling for 3D-Stacked ICs
Mottaqiallah Taouil, Said Hamdioui – TU Delft, NL; Erik Jan Marinissen – IMEC, BE

Poster 2: Standardization Working Group on 3D-Test / Project P1838
Erik Jan Marinissen – IMEC, BE; Adam Cron – Synopsys, USA

Poster 3: What Could be Hiding in Your 3D Silicon? Trojans and Counterfeits May Be Lurking in the 3D Stack
Jennifer Dworak – Southern Methodist University, USA; Al Crouch – Asset Intertech, USA

Poster 4: Wideband Ultralow Impedance Evaluation System of Power Distribution Network for Decoupling Capacitor Embedded Interposers of 3-D Integrated LSIs

Table-Top Demos

Table-top demos are on display throughout the workshop.

Dedicated demo sessions
- Thursday September 22: 18:30-19:00h
- Friday September 23: 10:00-10:30h and 13:00-13:30h

Demo 1: DFT Insertion and Interconnect TG for 3D Stacked ICs
Brion Keller – Cadence Design Systems, USA

Demo 2: IEEE 1149.1-2011, multi-TAP iMajik and Concurrent JTAG for 3D-SICs
Brian Turmelie, Craig Stephen – Intellitech, USA

Demo 3: Moving IC Test in a New Direction
Steve Paleras – Mentor Graphics, USA

Demo 4: New Publications from Springer of Interest to Attendees of 3D-TEST Workshop
Charles Glaser – Springer, USA

Demo 5: Synthesis-Based Test for 3D-IC
Adam Cron – Synopsys, USA

Demo 6: Cost Trade Off Analysis Tools
E. Jan Vardaman – TechSearch International, USA

For more information: http://3dtest.tttc-events.org

Corporate Supporters

The 3D-TEST Workshop gratefully acknowledges the financial support from the following companies:

- Advantest
- Cadence
- Mentor Graphics
- MicroProbe
- Synopsys
- Syntest
- Tokyo Electron