The 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs). While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Workshop Program – The workshop program contains the following elements.
- Keynote Address: “The Evolution of 3-D ICs: The Road to Production of a 6.8B Transistor FPGA” by Ivo Bolsens, CTO at Xilinx.
- Keynote address: “3D Integration: TSV and the Impact on DfT” by Stephane Lecomte, Member of Test Engineering Technical Staff at ST-Ericsson.
- Invited Address: “3D-Driven System Design – Present and Future” by Paul Franzon, Professor at North-Carolina State University.
- Five sessions with in total 14 paper presentations.
- Continuous display of posters and table-top demos.
- Panel discussion with market analysts, editors, and bloggers on “The 3D Buzz: Hype versus Reality”.

For the detailed version of the program, please turn over.

Participation – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes all technical sessions, Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as far as made available by their presenters), workshop reception, continental breakfast, lunch, and break refreshments. On-line registration is available via the workshop’s website (http://3dtest.tttc-events.org). Alternatively, register on-site during Test Week at the ITC Registration Counter at the Disneyland Hotel; admission for on-site registrants is subject to availability.

Further Information
Yervant Zorian  
General Chair
Synopsys
700 E. Middlefield Rd.
Mountain View, CA, USA
tel. +1 (650) 584-7120
yervant.zorian@synopsys.com

Erik Jan Marinissen  
Program Chair
IMEC
Kapeldreef 75
B-3001 Leuven, Belgium
tel. +32 (0)16 28-8755
erik.jan.marinissen@imec.be

Said Hamdioui  
Program Chair
Delft University of Technology
Mekelweg 4
2628CD, Delft, the Netherlands
tel. +31 (0)15 278-3643
s.hamdioui@tudelft.nl
Thursday November 8, 2012

Session 1: Opening – 1
Moderator: Saman Astham – TSMC, CAN
16:00h: Welcome Address
General Chair: Yervant Zorian – Synopsys, USA
Program Chairs: Erik Jan Marinissen – IMEC, BE
Sayd Hamdioui – TU Delft, NL
16:15h: Keynote Address:
The Evolution of 3D ICs: The Road to Production of a 6.8B Transistor FPGA
Ivo Bolsens – Xilinx, USA
16:45h: Invited Address:
3D-Driven System Design – Present and Future
Paul Franzen – NCSU, USA
After years of research and development, Through-Silicon Vias (TSVs) are becoming a manufacturing reality. Soon, a wave of new TSV-based 3D stacked ICs (and “2.5G” stacked ICs) will hit the market, including CMOS image sensors, memory cubes, stacked FPGA, and memory-on-logic. This will be followed by a set of more sophisticated products likely to have a focus on heterogeneous integration. For digital systems, one particularly benefit for going into the third dimension is reduced power consumption. However, to justify the investment it must be possible to achieve power savings of 25% or more. This cannot be achieved solely through shorter wires! 3D-specific design solutions are needed. A particular complexity in 3D integration is that designs that might be assembled into a 3D stack are likely to be designed at different times and places. This creates the need for common interface IP and interchange standards. The requirements and progress towards these will be presented and discussed.

Session 2: 3D Design-for-Test
Moderator: Michael Laisne – Qualcomm Technologies, USA
17:15h: Design for Testing 3D-TSVs Connecting Logic Die and Memory Die
Jing Ye, Yu Hu, Xiaowei Li – Chinese Academy of Sciences, CN;
Ruffeng Guo, Wu-Tung Cheng, Yu Huang, Liyang Lei – Mentor Graphics, USA
17:40h: Post-Test Insertion Retiming for TSV Boundary Cell in 3D ICs
Brandon Noia, Krishnendu Chakrabarty – Duke University, USA
18:05h: A Low-Overhead Method for Pre-Bond Test of Resonant 3-D Clock Distribution Networks
Somayyeh Rahimian, Vasillis F. Pavlidis, Giovanni De Michele – EPFL, CH

Session 3: Posters and Demos
18:30h: For list of Posters and Table-Top Demos: see next page.

Workshop Reception
19:00-21:00h

Friday November 9, 2012

Workshop Breakfast
07:00-08:00h

Session 4: Opening – 2
Moderator: Amy Leong – MicroProbe, USA
08:00h: Keynote Address:
3D Integration: TSV and the Impact on DIT
Stephanie Lecomte – ST-Ericsson, FR
3D die-to-die stacking has received a lot of attention recently, as it opens the door to integration of heterogeneous technologies. Among the first challenges were the setup of a viable Through-Silicon Via (TSV) technology module, and efficient die stacking and manufacturing processes. Design-for-Test (DfT) requirements had to evolve, to address new challenges on TSVs, top-of-die access, and die-to-die interconnect coverage. This talk discusses how innovative new DfT solutions really need to be, in view of short-term 3D applications. We review a few 3D examples made by ST and ST-Ericsson and their potential future applications in the smartphone market.

Session 5: 3D Wafer Probing
Moderator: Daniel Rishavy – TEL Test Systems, USA
08:30h: 40µm Pitch Probing Cu Pillar and Aluminum Pad
Joseph Foerstel – Altera, USA; Amy Leong – MicroProbe, USA

Session 6: 3D Electronic Design Automation
Moderator: Mike Ricchetti – AMD, USA
09:20h: Extension of a 3D-DIT Architecture for Embedded Cores and Multiple Towers
Briana Kelter, Christos Papametale, Vivek Chickermane – Cadence Design Systems, USA;
Erik Jan Marinissen – IMEC, BE
09:45h: An EDA Approach to 3D-IC DIT Requirements
Etienne Racine, Ron Press, Rick Fisette, Martin Keim – Mentor Graphics, USA
10:10h: An Effective Infrastructure IP for Memory Dies in 3D-ICs
Yervant Zorian, Gurgen Harutyunyan – Synopsys, USA

Session 7: Posters and Demos
10:35h: For list of Posters and Table-Top Demos: see next page.
Coffee and tea provided.

Session 8: Editor’s Panel Discussion
10:50h: The 3D Buzz: Hype versus Reality
Moderator: Françoise von Trapp – Queen of 3D, Founder/Director 3D Incites, USA
Panelists: Ira Feldman – Principal Consultant, Feldman Engineering Corp., USA
Herb Reiter – President, eda2asic, USA
Jan Vardaman – CEO, TechSearch International, Inc., USA
Paul Werbaneth – Executive Consultant, Semiconductor Technology Associates, USA
You’ve read their market reports and columns, attended their presentations, subscribed to their blogs, and followed them on LinkedIn an Twitter. They may not be the ones making the manufacturing decisions about when to implement 3D technologies, but they certainly do their part in influencing key decision makers in semiconductor device manufacturing, guiding them on path to 2.5D and 3D ICs through their analysis, research, news and observations. They are the analysis and journalism who have been following different aspects of the 3D story for years. We’ve gathered four of them to share their perspective on what’s hype and what’s reality in the march towards commercialization of 3D ICs.

Workshop Luncheon
12:00-13:00h

Session 9: Posters and Demos
13:00h: For list of Posters and Table-Top Demos: see next page.

Session 10: 3D Cost Modelling and Yield
Moderator: Michael Higgins – Analog Devices, IRL
13:30h: The Implications of Fault Toleration for Yield, Known Good Die, and Test Strategies in 3D Integration
Kenneth Rose, Adam Beece, Tong Zhang, James Lu – Rensselaer Polytechnic Institute, USA
13:55h: 3D-COSTAR: A Cost Model For 3D Stacked ICs
Mottaghalia Taouil, Sayd Hamdioui – TU Delft, NL;
Erik Jan Marinissen – IMEC, BE; Sudipta Bhowmik – Qualcomm, USA

Session 11: 3D Test Quality and Failure Analysis
Moderator: Shi-Yu Huang – National Tsing-Hua University, TW
14:20h: Testing of TSV-Induced Small Delay Faults for Three-Dimensional Integrated Circuits
Chun-Yi Kuo, Chi-Jih Shih, Yi-Chang Lu, James C.-M. Li – National Taiwan University, TW;
Krishnendu Chakrabarty – Duke University, USA
14:45h: TSV Stress-Aware ATPG for 3D Stacked ICs
Sergej Deutsch, Krishnendu Chakrabarty – Duke University, USA;
Shreepad Panth, Sung Kyu Lim – Georgia Tech, USA
15:10h: Application of Lock-In Thermography as a First Step in the 3D Failure Analysis Workflow of System-in-Packages
Kannu Wadhwa – DCG Systems, USA;
Christian Schmidt, Frank Altmann – Fraunhofer IWM, Germany
15:35h: Workshop Closure
Posters and Table-Top Demos

**Posters**

Posters are on display throughout the workshop. Dedicated poster sessions:
- Thursday November 8: 18:30-19:00h
- Friday November 9: 10:30-10:45h and 13:00-13:20h

Poster 1: Optimization of MEMS-IC SiP Development Reliable Design Methods
Grzegorz Janczyk, Tomasz Bieniek – Instytut Technologii Elektronowej, PL

Poster 2: Standardization Working Group on 3D-Test / Project P1838
Erik Jan Marinissen – IMEC, BE; Adam Cron – Synopsys, USA

Vladimir Zheleznyak, Dima Gobuslavsky – Camtek, IL

Poster 4: Reliability Investigation by Examination of Dedicated MEMS/ASIC and NW’s Test Structures Related to Novel 3D SiP and Nano-Sensors Systems
Tomasz Bieniek, Grzegorz Janczyk – Instytut Technologii Elektronowej, PL

**Table-Top Demos**

Table-top demos are on display throughout the workshop. Dedicated demo sessions:
- Thursday November 8: 18:30-19:00h
- Friday November 9: 10:30-10:45h and 13:00-13:20h

Demo 1: New IEEE P1149.1-2013 supports SoCs with stacked WideIO Memory
CJ Clark, Brian Tumelle, Craig Stephan – Intellitech, USA

Demo 2: New Publications from Springer of Interest to Attendees of 3D-TEST Workshop
Charles Glaser – Springer, USA

For more information: [http://3dtest.tttc-events.org](http://3dtest.tttc-events.org)

**Corporate Supporters**

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