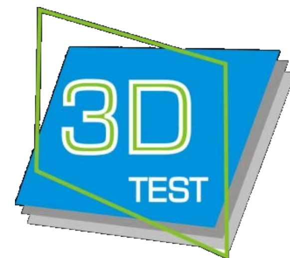
Fourth IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

3D-TEST



in conjunction with ITC / Test Week 2013
Disneyland Hotel – Anaheim, California, USA
September 12+13, 2013
http://3dtest.tttc-events.org

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Call for Participation

The 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs), micro-bumps, and/or interposers. While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Workshop Program – The workshop program contains the following elements.

- Keynote Address: "3D Solutions in the Coming Age of Terabit Communication" by Nicholas Ilyadis, VP and CTO at Broadcom.
- Four sessions with in total 11 paper presentations.
- Two panel-discussion sessions
  - On "Requirements for 3D Volume Production Testing"
  - On "How Will 3D-Testing Change the Test Supply Chain?"
- A special session with presentations by and discussions with nominees of the 2013 3DInCites Award in the category Test & Reliability Tools and Equipment.
- Continuous display of table-top demos.

For the detailed version of the program, please turn over.

Participation – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes access to all technical sessions, Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as made available by their presenters), workshop reception, continental breakfast, lunch, and break refreshments. On-line registration is available via the workshop's website (http://3dtest.tttc-events.org). Alternatively, register on-site during Test Week at the ITC Registration Counter at the Disneyland Hotel; admission for on-site registrants is subject to availability.

Further Information

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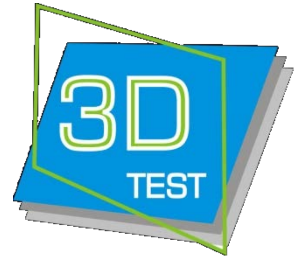

Preliminary Workshop Program

Thursday September 12, 2013

Session 1: Opening

Moderator: Rafic Zein Makki – GlobalFoundries, USA

16:30h: **Welcome Address**
General Chair: Yervant Zorian – Synopsys, USA
Program Chair: Erik Jan Marinissen – IMEC, BE

16:45h: **Keynote Address**:
3D Solutions In the Coming Age of Terabit Communication
Nicholas Ilyadis – VP and CTO, Broadcom Infrastructure & Networking, USA

As Ethernet switching approaches terabit levels of overall throughput, new paradigms are emerging, along with solutions that encompass 3D fabrication and packaging technologies. TSV/TSI's, memory stacks, wafer bonding, heterogeneous device packaging and silicon photonics are driving overall system capacity to new levels. At the same time, these technologies are creating challenges in device testing and yield, downstream final assembly and test, and overall system reliability and serviceability. This talk will target an audience of production and test engineers, exploring technology drivers for 3D solutions and highlighting unique challenges introduced by the progression toward terabit-level communications.

Session 2: Table-Top Demos

17:30h: For list of Table-Top Demos: see next page.

Session 3: Panel Discussion

18:00h: **Requirements for 3D Volume Production Testing**

Moderator: Bill Eklow – Cisco Systems, USA

Panelists: *Saman Adham – Senior Manager – TSMC, CAN*
Amer Cassier – Senior Product Engineer – Qualcomm, USA
Manuel d'Abreu – Engineering Fellow – SanDisk, USA
Amit Majumdar – Principal Engineer – Xilinx, USA
Mike Ricchetti – Fellow Design Engineer – AMD, USA

As the industry prepares for commercialization of 3D ICs, test requirements will vary based on the device being manufactured, and the manufacturer of that device. Panelists from various sectors of semiconductor manufacturing including memory, logic, foundries, and fabless will share their requirements with the test community and answer critical questions. Topics include defect detection, design-for-test, test equipment, and test costs.

Workshop Reception

19:30-21:30h

Friday September 13, 2013

Workshop Breakfast

07:00-08:00h

Session 4: Test Flow and Yield Optimization

Moderator: James C.-Mo. Li – National Taiwan University, TW

08:00h: Exploiting Sector-on-Sector Stacking for Yield Improvement of 3D ICs
Bei Zhang, Baohu Li, Vishwani Agrawal – Auburn University, USA

08:25h: 3D Test Flow Modeling and Verification
Armin Grünewald, Michael Wahl, Kai Hahn, Rainer Brück – Univ. Siegen, DE

Session 5: Power to 3D-Test!

Moderator: Marc Loranger - FormFactor, USA

08:50h: 3D IC Test Through Power Line Methodology
Alberto Pagani, Alessandro Motta – STMicroelectronics, IT

09:15h: In-Place Signal and Power Noise Waveform Capturing Within 3D Chip Stacking
Makoto Nagata, Satoshi Takaya – Kobe Univ., JP;
Hiroaki Ikeda – ASET, JP

09:40h: Testing Leakage Faults of Power TSV in 3D IC
Chi-Hih Shih, Shih-An Hsieh, Yi-Chang Lu, James C.-M. Li, Tzong-Lin Wu – National Taiwan Univ., TW; Krishnendu Chakrabarty – Duke University, USA

Session 6: Table-Top Demos

10:05h: For list of Table-Top Demos: see next page.
Coffee and tea provided.

Session 7: 3D Wafer Probing

Moderator: Marc Hutner – Teradyne, US

10:30h: Signal Integrity Design for Wide IO and 3D-TSV IC Test at Wafer Probe
Ken Smith, Daniel Bock – Cascade Microtech, USA

10:55h: Very Low Damage Direct Testing of Micro-Bumps for 3D IC Integration
Onnik Yaglioglu, Ben Eldridge – FormFactor, USA;
Shoji Wada – Elpida Memory, JP

Session 8: Panel Discussion

11:20h: **How Will 3D-Testing Change the Test Supply Chain?**

Moderator: tbd

Panelists: *Adam Cron – Principal Engineer – Synopsys, USA*
Gary Fleeman – VP of Marketing – Advantest, USA
Gerard John – Technical Director Test Development – Amkor, USA
TM Mak – Director 2.5D/3D DfT Strategy – GlobalFoundries, USA
Erik Jan Marinissen – Principal Scientist – IMEC, BE
Daniel Rishavy – Principal Product Manager – TEL Test Systems, USA

3D IC stacking is more intricate than 2D assembly and requires elaborate testers to perform fully functional test. Built-in self-test adds cost and takes die real estate. Going to 3D means re-thinking the test strategy from what it was in the past, especially in terms of economics. Panelists from across the test value chain will discuss strategies to address the unique circumstances surrounding 3D IC testing.

Workshop Luncheon

12:20-13:20h

Session 9: 3D Design-for-Test

Moderator: Kun Young Chung – Samsung, KR

13:20h: 3D Design-for-Test Architectures Based on IEEE P1687
Yassine Fkih, Pascal Vivet – CEA-Leti, FR; Bruno Rouzeyre, Marie-Lise Flottes, Giorgio Di Natale – LIRMM, FR; Jürgen Schlöffel – Mentor Graphics, DE

13:45h: Development of Testing Technology for Wide Bus Chip-to-Chip Interconnection in 3D LSI Chip Stacking System
Masahiro Aoyagi, Fumito Imura, Samson Melamed, Shunsuke Nemoto, Naoya Watanabe, Katsuya Kikuchi, Hiroshi Nakagawa – AIST, JP;
Michiya Hagimoto, Yuko Matsumoto – TOPS Systems Corporation, JP

14:10h: Expandable and Reliable 2.5D SOC Design with Reconfigurable Logic Dies
Li Jiang, Feng Yuan, Qiang Xu – Chinese Univ. of Hong Kong, HK;
Bill Eklow – Cisco Systems, USA

14:35h: TSVs Pre-Bond Testing: A Test Scheme for Capturing BIST Responses Under PVT Variations
Marie-Lise Flottes, Giorgio Di Natale, Bruno Rouzeyre, Hakim Zimouche – LIRMM, FR

Session 10: Special Session on 2013 3DInCites Awards

15:00h: **Nominees in the Category Test & Reliability Tools and Equipment**

Moderator: Françoise von Trapp – « Queen of 3D », Founder/Director 3DInCites, USA

Nominees: *Encounter Test: Brion Keller – Cadence Design Systems, USA*
Tessent MemoryBIST: Steve Pateras – Mentor Graphics, USA
CM300 Probe Station: Ken Smith – Cascade Microtech, USA
NanoPierce Contactor: Mike Slessor – FormFactor, USA
InStrip3D: Tbd – Multitest, USA
NSX320 Metrology Series: David Marx – Rudolph Technologies, USA

This Special Session features the nominees and the winner of the 2013 3DInCites Awards' Test and Reliability Tools and Equipment category. Moderated by Françoise von Trapp (Queen of 3D), each panelist will briefly introduce the product that was nominated for the award, and discuss the technical merits. The remainder of the session will be in a Q&A discussion format, focused on these innovative solutions for 3D IC test and reliability including design-for-test solutions, probe card and test contactor technology, built-in-self test for memory, test handlers, and inspection and metrology for TSV reliability.

16:00h: Workshop Closure

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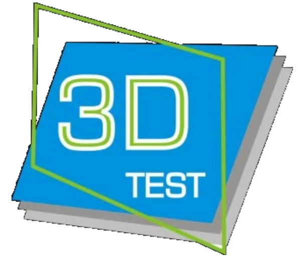

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Table-Top Demos

Table-Top Demos

Table-Top Demos are on display throughout the workshop.
Dedicated demo sessions

- Thursday September 12: 17:00-17:30h
- Friday September 13: 10:05-10:30h

Demo 1: An Innovative Method for 2.5D/3D IC Interconnection Integrity Monitoring
Hans Manhaeve – Ridgetop Europe, BE; Andrew Levy – Ridgetop Group, USA; Chih-Yang Li – ALLVia, USA
Demo 2: Pyramid Probe Card
Ken Smith – Cascade Microtech, USA
Demo 3: IEEE 1149.1-2013 Support for 3D Stacked Die
Brian Turmelle, Craig Stephan, CJ Clark – Intellitech, USA
Demo 4: Synopsys Synthesis-Based 3D-IC Test
Avetik Yessayan, Yervant Zorian, Adam Cron – Synopsys, USA
Demo 5: 40µm Pitch Probe Card Solution
Marc Loranger, Onnik Yaglioglu, Amy Leong – FormFactor, USA

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