JETTA – Special Issue on Testing Three-Dimensional Stacked Integrated Circuits

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Vertical stacking of multiple integrated circuits (such as System-in-Package and Package-on-Package) offers dense integration of possibly heterogeneous technologies with a small area footprint. The semiconductor industry is preparing itself now for vertical interconnection of multiple stacked tiers by means of Through-Silicon Vias (TSVs) in so-called 3D-SICs. In comparison to conventional wire-bonded interconnects, TSVs promise to increase the interconnect bandwidth and performance while lowering power dissipation and overall manufacturing cost. Consequently, TSV-based 3D technologies enable the creation of a new generation of 'super chips' by opening up new architectural opportunities and hence might help the semiconductor industry to extend the momentum of Moore's Law into the next decade.

Like all ICs, these new three-dimensional stacked ICs need to be tested for manufacturing defects, in order to guarantee sufficient outgoing product quality to the customer. Whereas 3D-SICs require most of today's advanced test and Design-for-Test (DfT) approaches, simply because they are composed of advanced IC designs in advanced technology nodes, they also have some unique test challenges of their own. These challenges, amongst others, pertain to test flows, test contents, and test access.

This JETTA Special Issue will contain papers on all test aspects of 3D-SICs. The topics of interest include, but are not limited to:

- Defects due to Wafer Thinning
- Defects in Intra-Stack Connects
- DfT Architectures for 3D-SICs
- EDA Design-to-Test Flow for 3D-SICS
- Failure Analysis for 3D-SICs
- Known-Good Die / Stack Testing
- Pre-Bond and Post-Bond Testing
- Reliability of 3D-SICs
- Standardization for 3D Testing
- System/Board Test Issues for 3D-SICs
- Test Cost Modeling for 3D-SICs
- Test Flow Optimization for 3D-SICs
- Tester Architecture, incl. ATE and BIST
- Thermal/Mechanical Stress in 3D-SICs
- TSV Test, Redundancy, and Repair
- Wafer Probing and Probe Damage of 3D-SICs

Authors should submit previously unpublished papers to the manuscript submission website http://www.editorialmanager.com/jetta/ specifying the article type as "3DTEST11". Expanded versions of conference papers (with at least 30% additional material) are also welcome. Please follow the author instructions available at http://www.springer.com/10836/ when submitting your paper. The final selection will be made through the journal's peer review process. The schedule is as follows:

Paper submission deadline:	December 15, 2010
Acceptance/rejection notification:	February 28, 2011
Final manuscript due:	March 31, 2011
Tentative publication date:	August 2011

Authors of papers accepted for the Special Issue will also be given the opportunity to expand their paper into a book chapter, to be included in a book on 3D-Testing Springer will publish later in 2011.

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