Benefits of Integrated System Design for complex FPGAs

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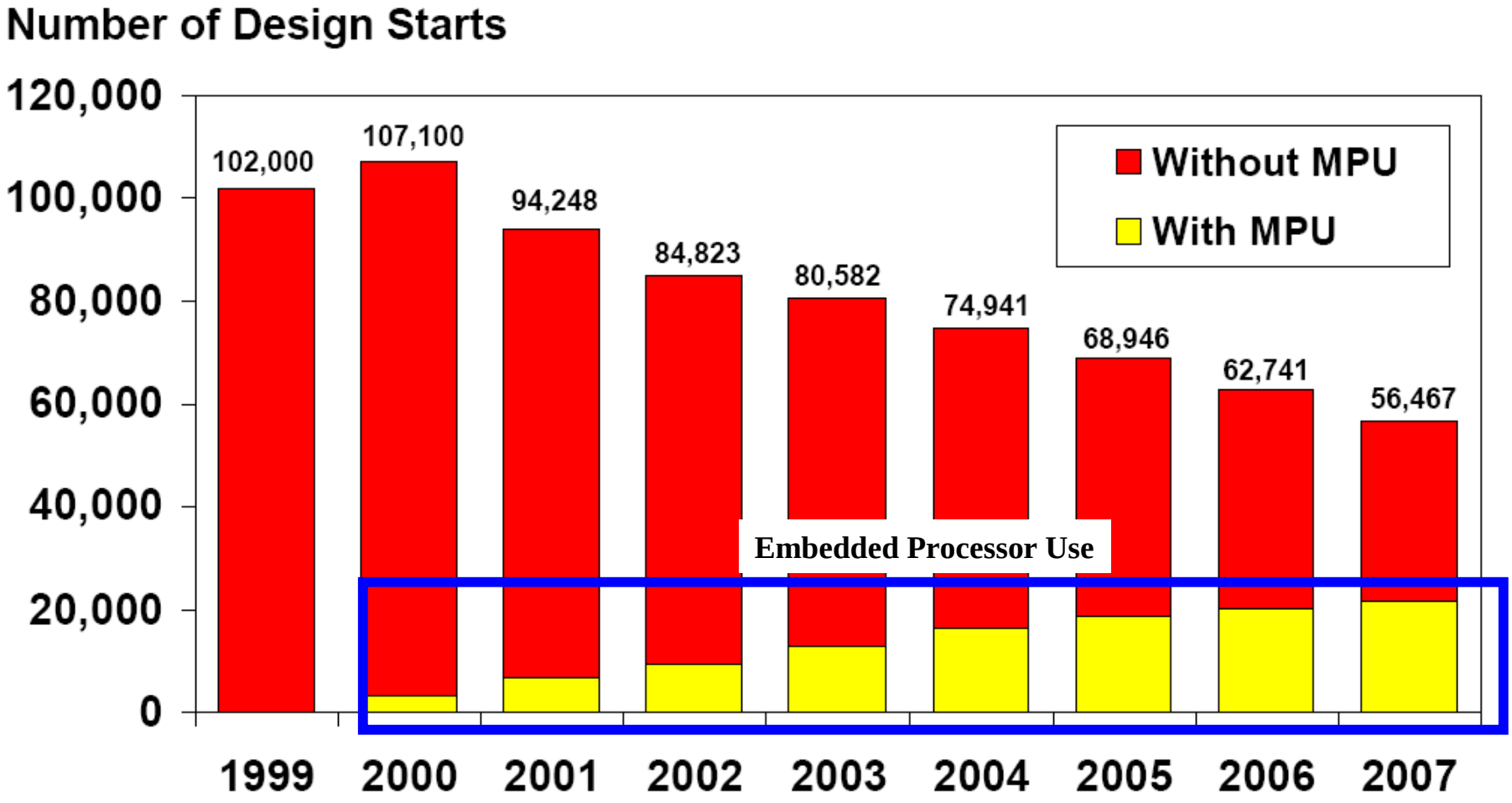
Mentor Graphics

Agenda

- FPGA/ASIC Trends
- Platform Based Design
- Optimizing Platform Performance
- Rapid Platform Prototyping
- Platform Design Verification
- Platform Example
- Summary

Trends - FPGA Design Starts



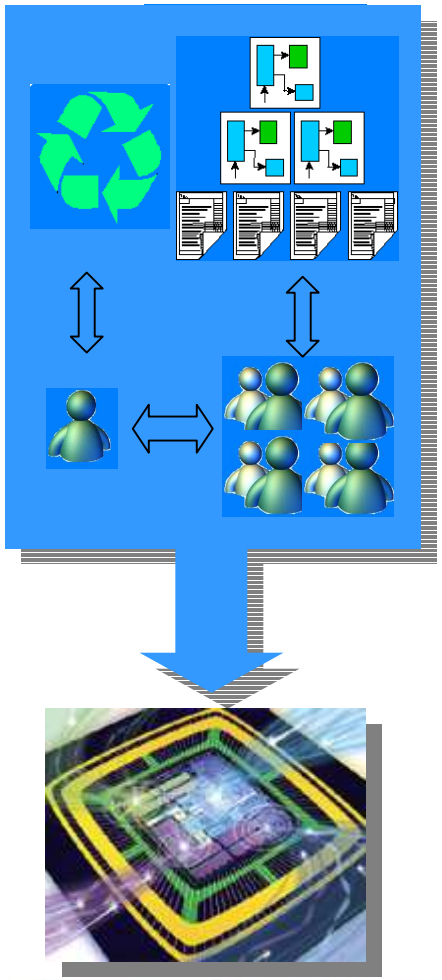
* Gartner Dataquest 2004 Trends – Brian Lewis

Embedded Microprocessor Use

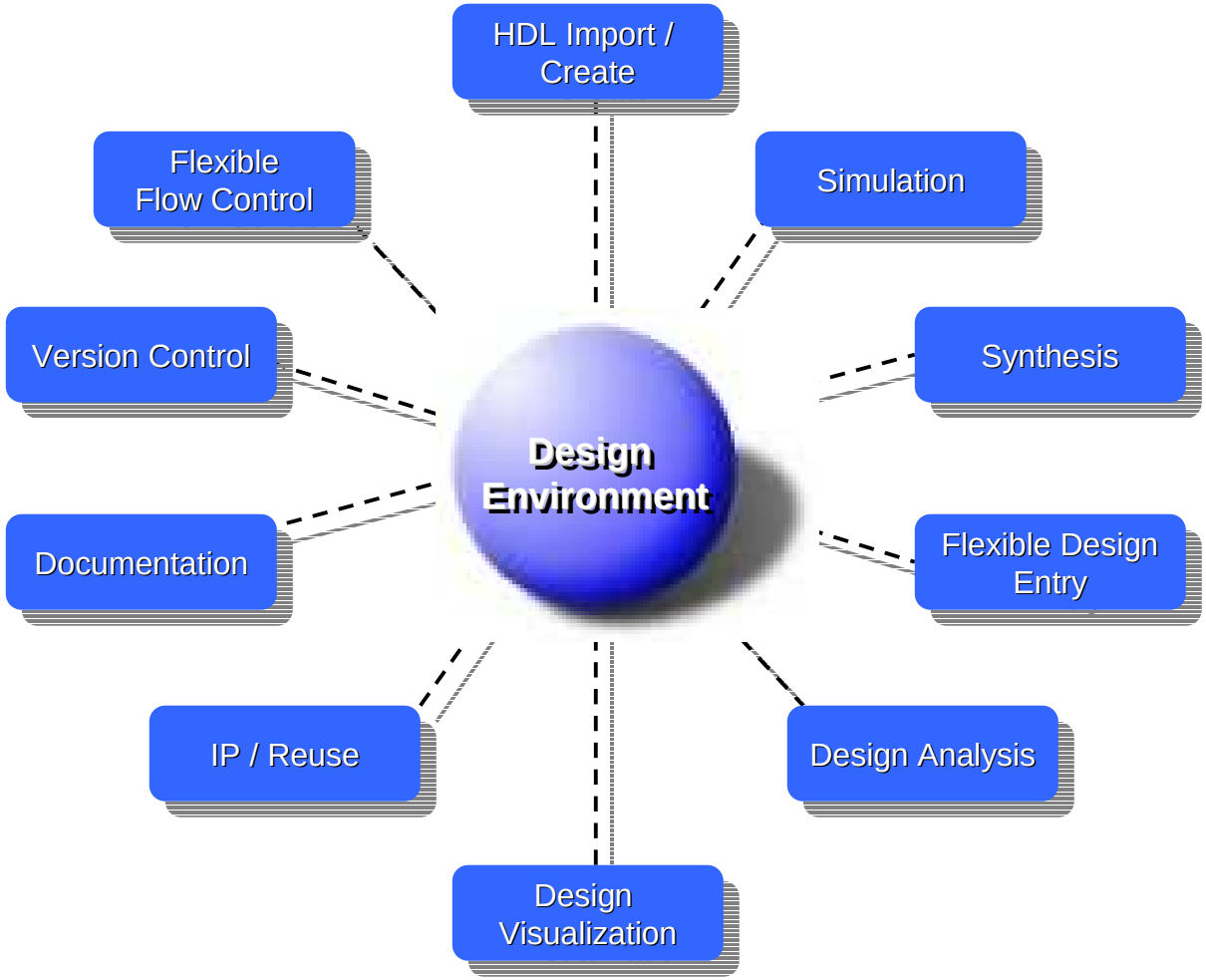
- **Rapid Growth for Embedded Processors in FPGA's**
  - **2003: 17%**
  - **2007: 37% (projected)**
- **Utilization of embedded processors and other embedded ASIC-macrocells in FPGAs enables:**
  - **High level of integration at the chip and PCB level**
  - **Reduced number of Components on PCB**
  - **Integrated System Design of the SOPCB**
- **But with all of this power comes complexity**
  - **More later…**

Platform Based Design

- **Traditional Platform Based Design**
  - **ASIC based**
    - **Use existing IP blocks**
      - **CPUs, high speed I/O's,**
      - **Pre-verified cores from core vendors**
  - **Keys to Platform Design Success**
    - **Design environment/solution that provides the following:**
      - **Predictable / Flexible Flow**
      - **Design Data Management**
      - **IP Reuse**
      - **Design Data Visualization**
      - **Version Control**
      - **Powerful Design Analysis**
      - **Accurate Design Documentation**



Design Environment for Platform Development



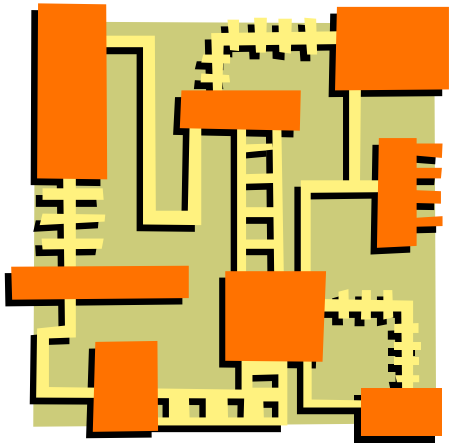
Platform Based FPGA Characteristics

- **Typical Characteristics**
  - **Embedded Processors**
    - **Hard / Soft – DSP, uController, uProcessor, etc**
  - **Complex Architecture Specific IP**
    - **High Quality – Tested and Qualified**
      - **Vendor Provided**
      - **3rd Party Provided (Mentor Inventra, etc)**
  - **Large Flexible Memory Blocks**
  - **High Speed I/Os**
    - **Gigabit speeds**
    - **Multiple signaling standard available per I/O pin**
  - **Multi-Million Gate Fabrics for User Logic**

Why Platform FPGAs?

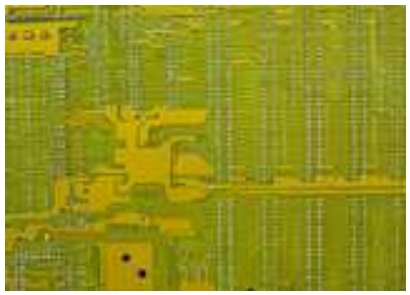
Discrete Component Implementation

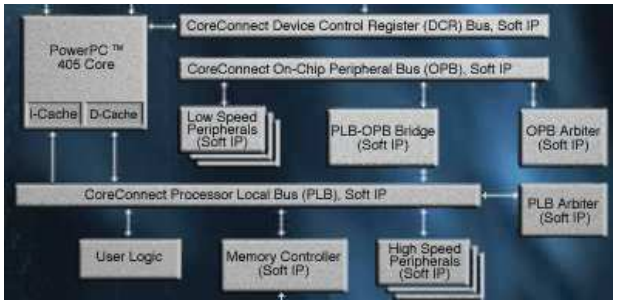
- Low Cost PCB
- Low Cost Components



Platform FPGA:

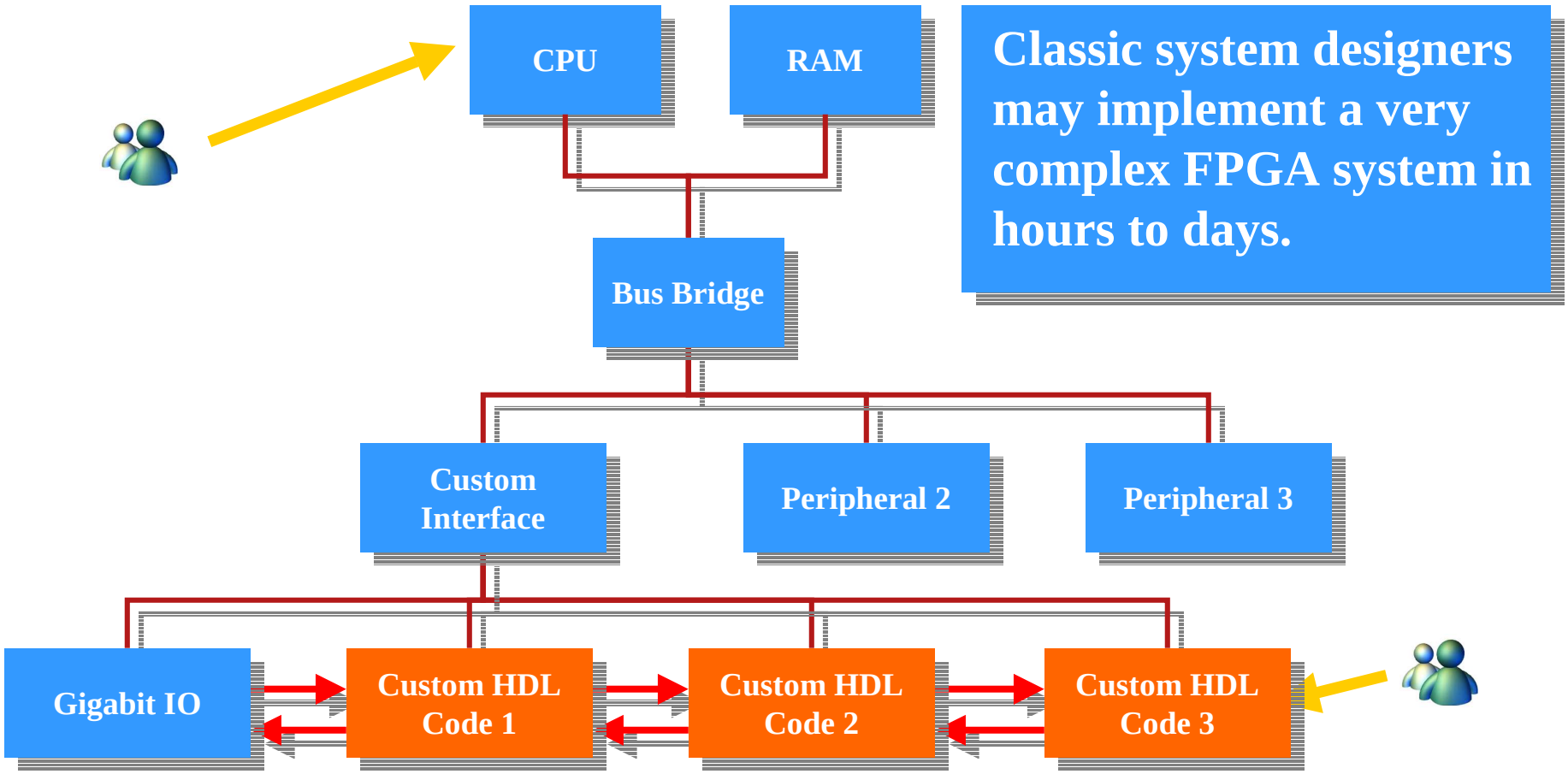
- High Cost HDI PCB
- High Cost Components





Why?

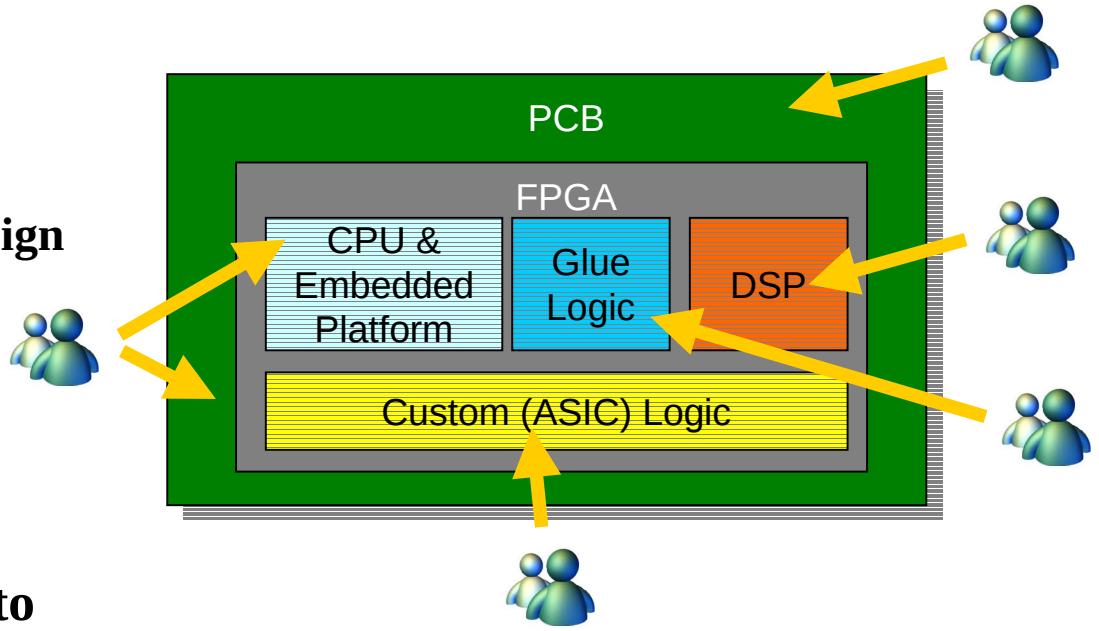
- **ASIC & System Integration + Flexibility!**



Classic system designers may implement a very complex FPGA system in hours to days.

…With Power Comes Complexity

- **Challenges of Design with Platform Based FPGAs**
  - **Merging of Multi-Disciplines of Individuals and Teams**
    - **System Level Design**
    - **Logic Design**
    - **PCB I/O Design**
    - **PCB Design**
  - **Optimizing the Platform Design**
    - **Performance**
    - **PCB Design**

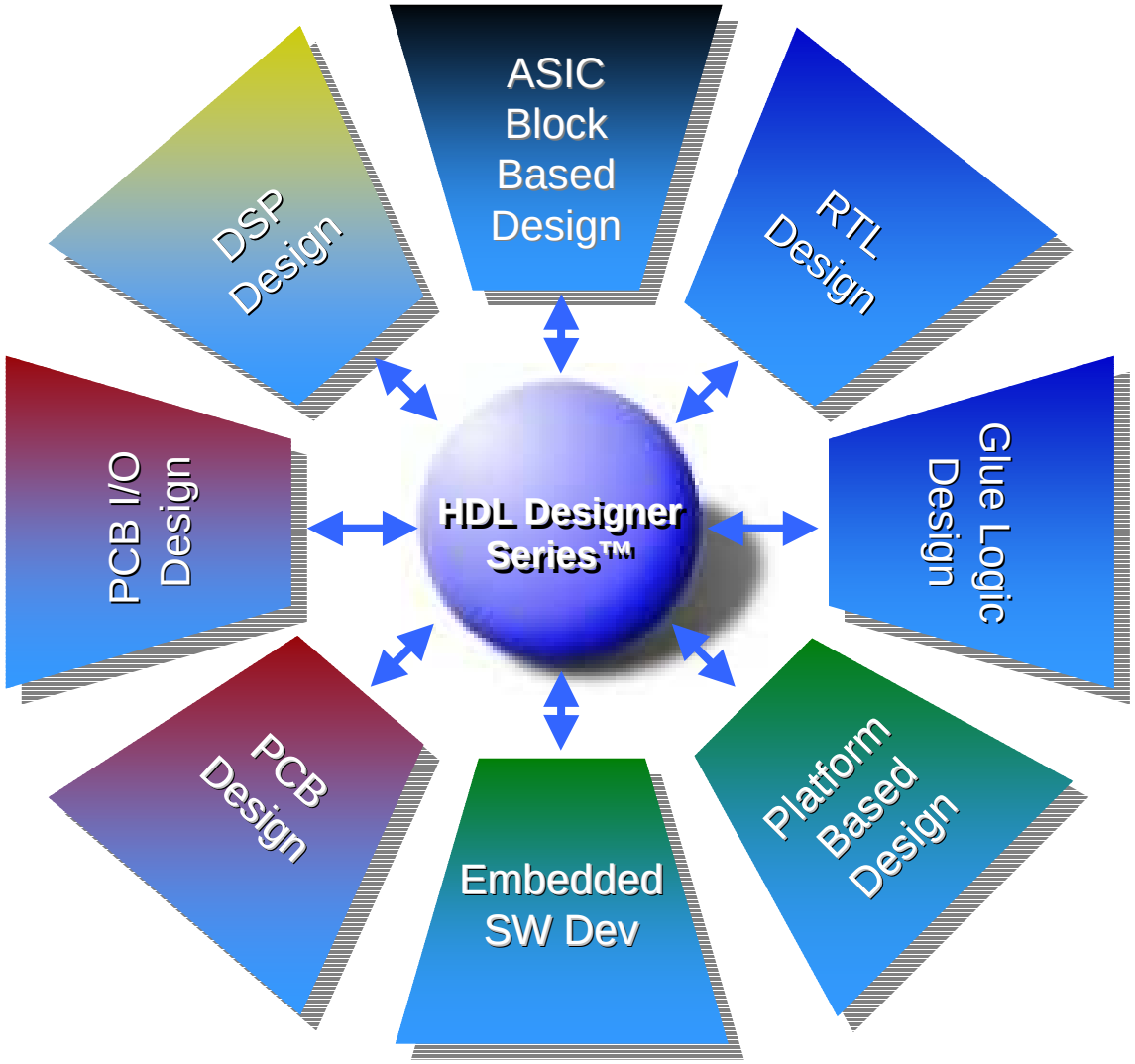


- **A design solution is required to**
  - **Maximize productivity across the disciplines**
  - **Optimize the platform design**
  - **Provide a highly organized and repeatable process**
  - **Enable team based design**
  - **Supports leading edge FPGA platform solutions**

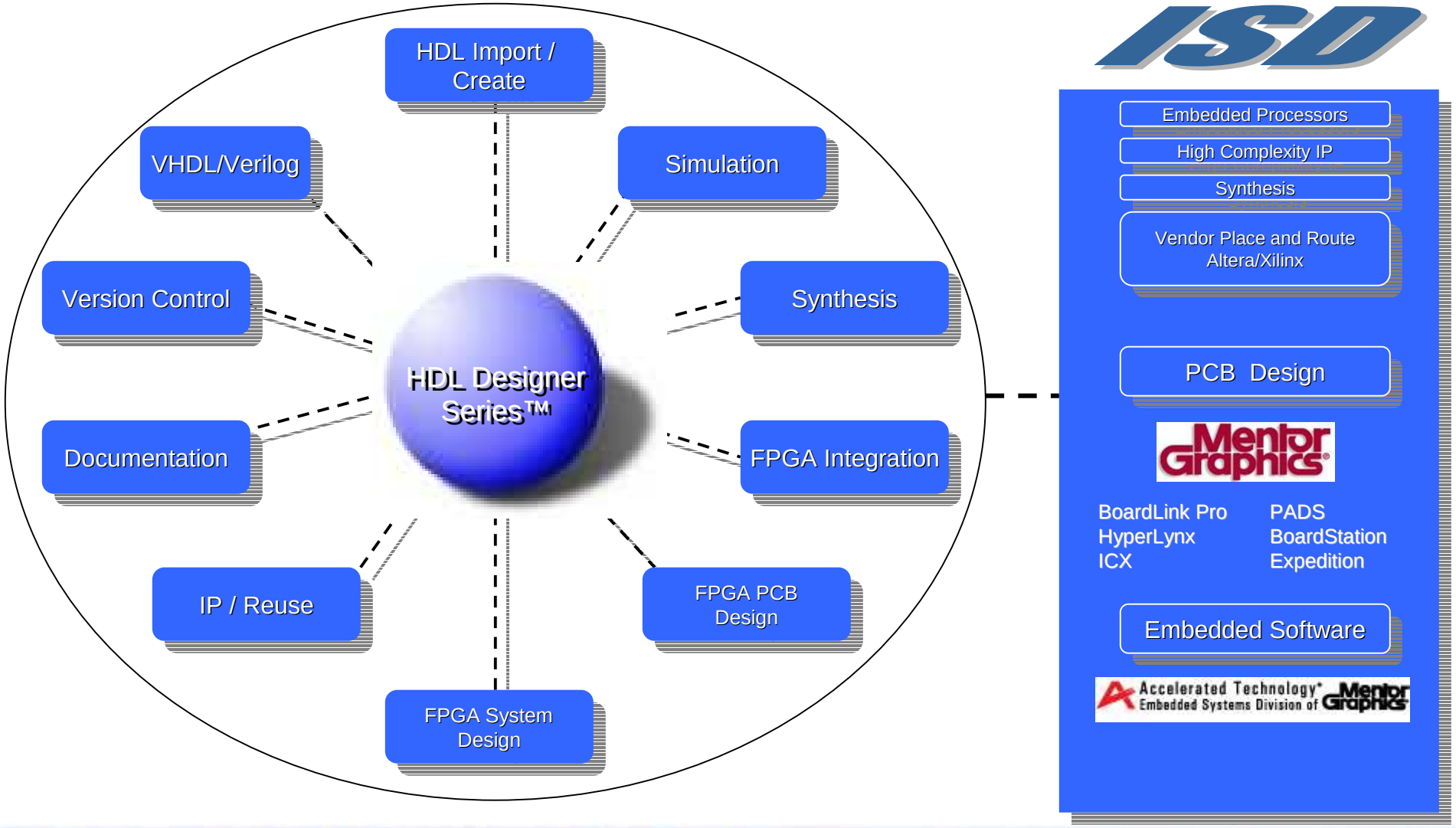
The Solution …

ISD
Integrated System Design

- **Harnessing the Power of Platform FPGAs with HDL Designer Series**

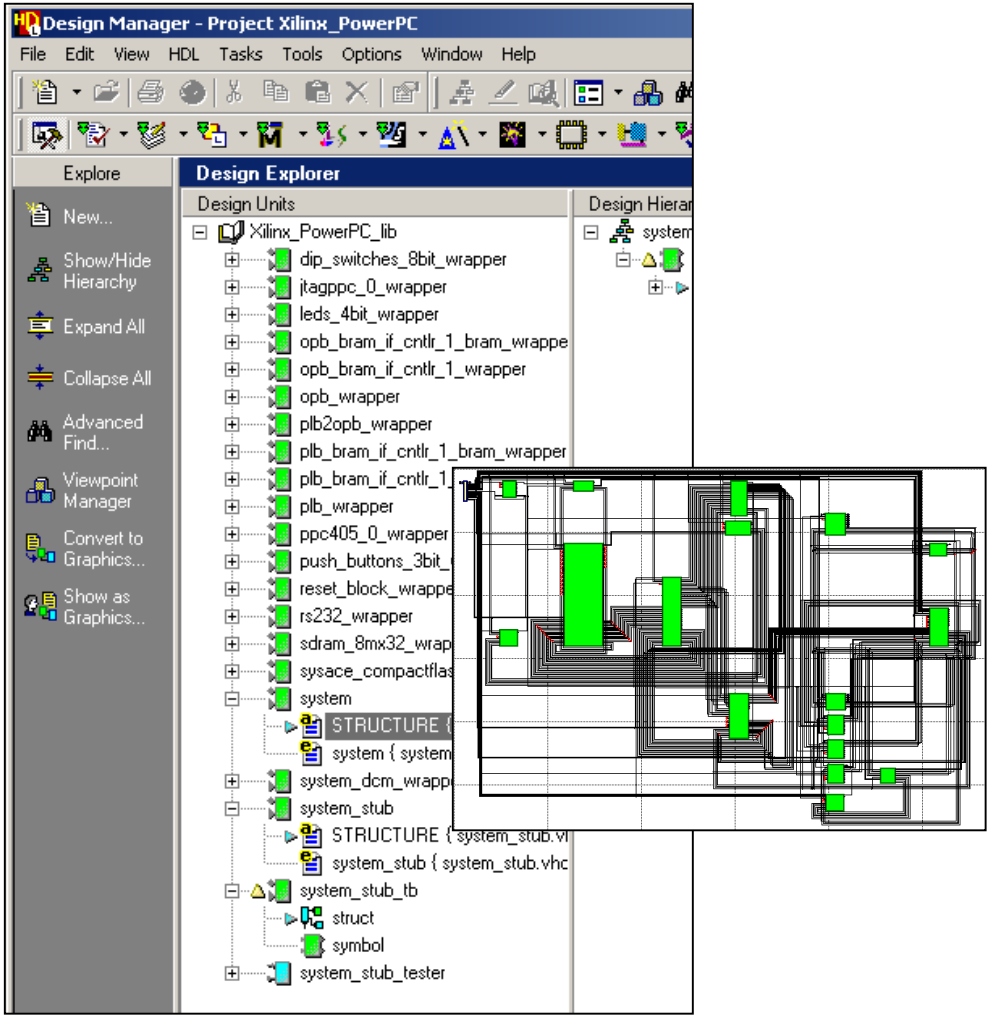


Integrated System Design



Quickly Understand Designs

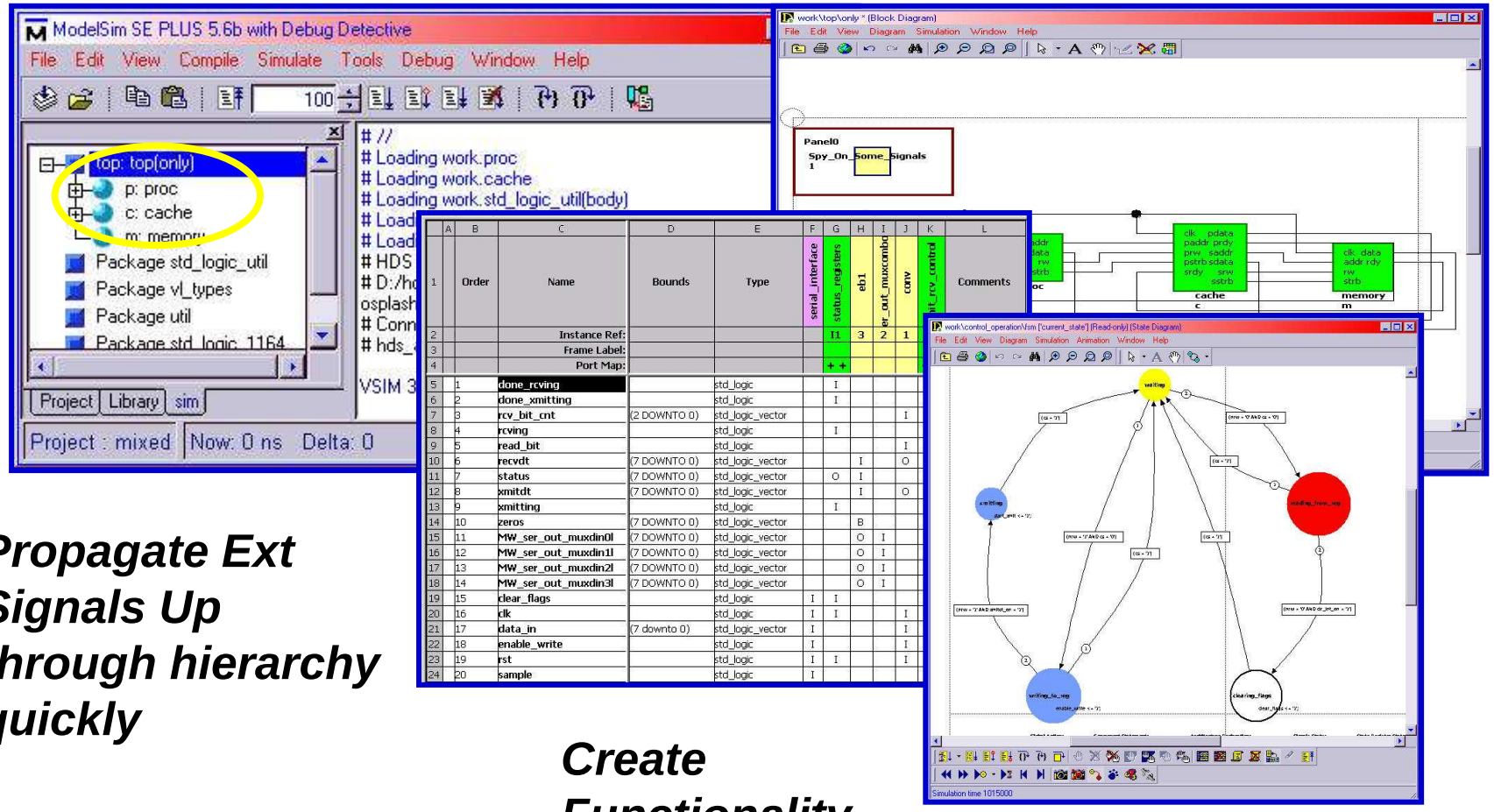
- **Logical information extracted automatically**
  - **HDL code parsed rapidly**
    - **Syntax errors highlighted**
  - **“Virtual” design units are created automatically**
    - **Shown in Design Units view**
    - **Logical content analyzed down to leaf level**
    - **Hierarchy shown selectively in separate pane**
  - **Easy design navigation**



Fast Custom Peripherals

Design Verification

Create Ext Signals



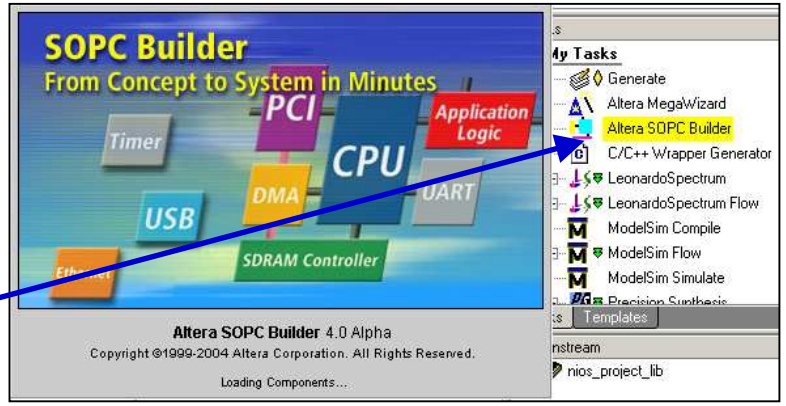
	Order	Name	Bounds	Type	serial_interface	status_registers	eb1	er_out_muxcombo	conv	Comments
2		Instance Ref:				I1	3	2	1	
3		Frame Label:								
4		Port Map:				+ +				
5	1	done_rcving		std_logic		I				
6	2	done_xmitting		std_logic		I				
7	3	rcv_bit_cnt	(2 DOWNTO 0)	std_logic_vector					I	
8	4	rcving		std_logic		I				
9	5	read_bit		std_logic					I	
10	6	recvdt	(7 DOWNTO 0)	std_logic_vector			I		O	
11	7	status	(7 DOWNTO 0)	std_logic_vector		O	I			
12	8	xmitdt	(7 DOWNTO 0)	std_logic_vector			I		O	
13	9	xmitting		std_logic		I				
14	10	zeros	(7 DOWNTO 0)	std_logic_vector			B			
15	11	MW_ser_out_muxdin0l	(7 DOWNTO 0)	std_logic_vector			O	I		
16	12	MW_ser_out_muxdin1l	(7 DOWNTO 0)	std_logic_vector			O	I		
17	13	MW_ser_out_muxdin2l	(7 DOWNTO 0)	std_logic_vector			O	I		
18	14	MW_ser_out_muxdin3l	(7 DOWNTO 0)	std_logic_vector			O	I		
19	15	clear_flags		std_logic	I	I				
20	16	clk		std_logic	I	I			I	
21	17	data_in	(7 downto 0)	std_logic_vector	I				I	
22	18	enable_write		std_logic	I				I	
23	19	rst		std_logic	I	I			I	
24	20	sample		std_logic	I					

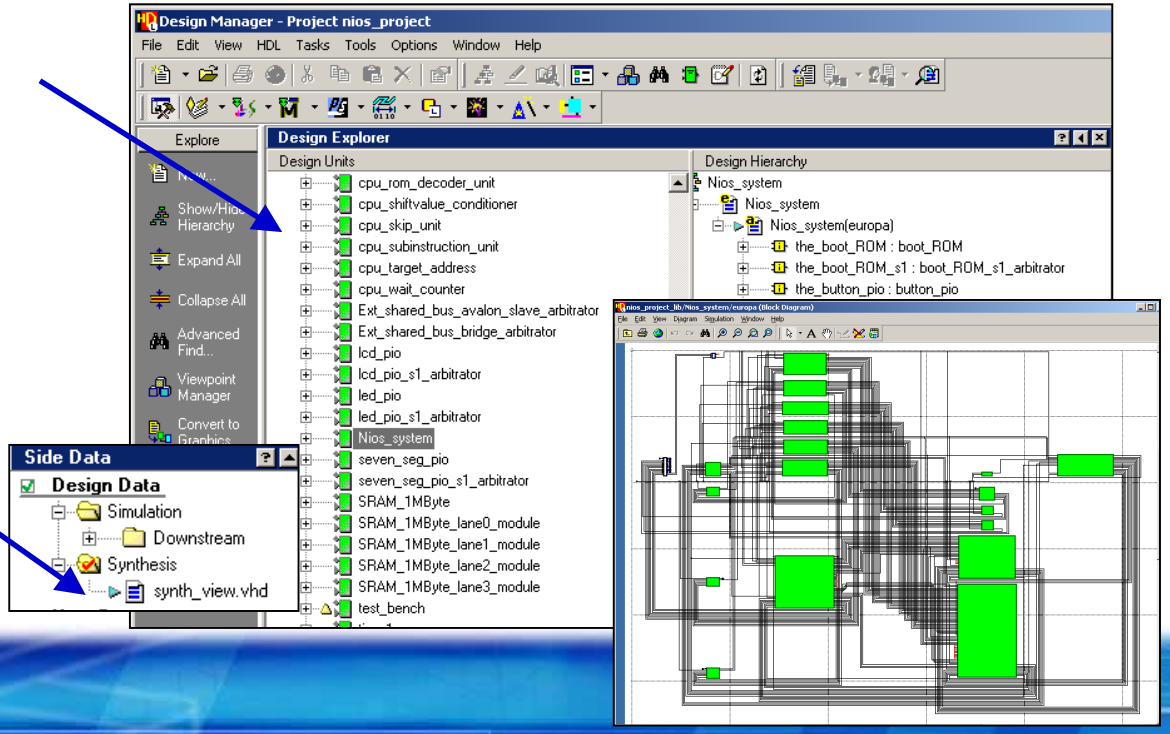
Propagate Ext Signals Up through hierarchy quickly

Create Functionality

Altera Nios Integration

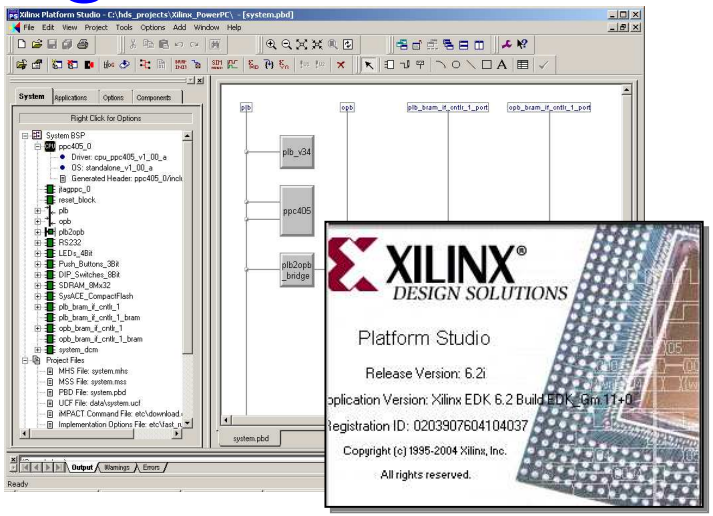
- Supports Nios 3.1 CPU
- QuartusII 4.0 integration
  - Easy SOPC Builder plugin
- Simulation View (ModelSim) HDS Design Browser
- Alternative Synthesis View for LeonardoSpectrum & Precision

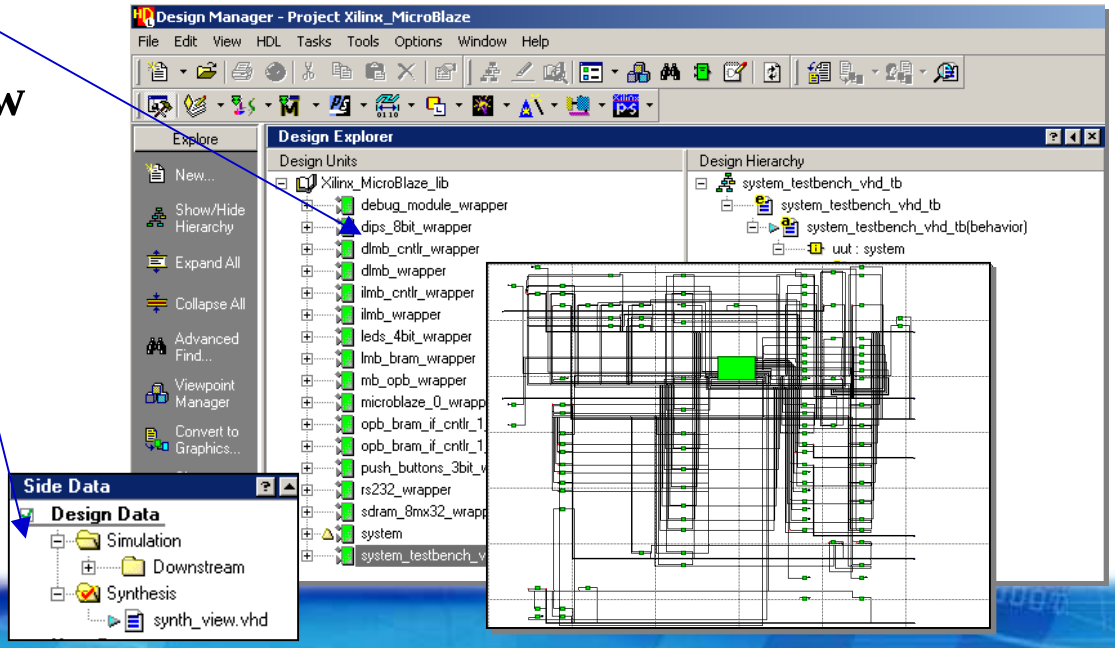




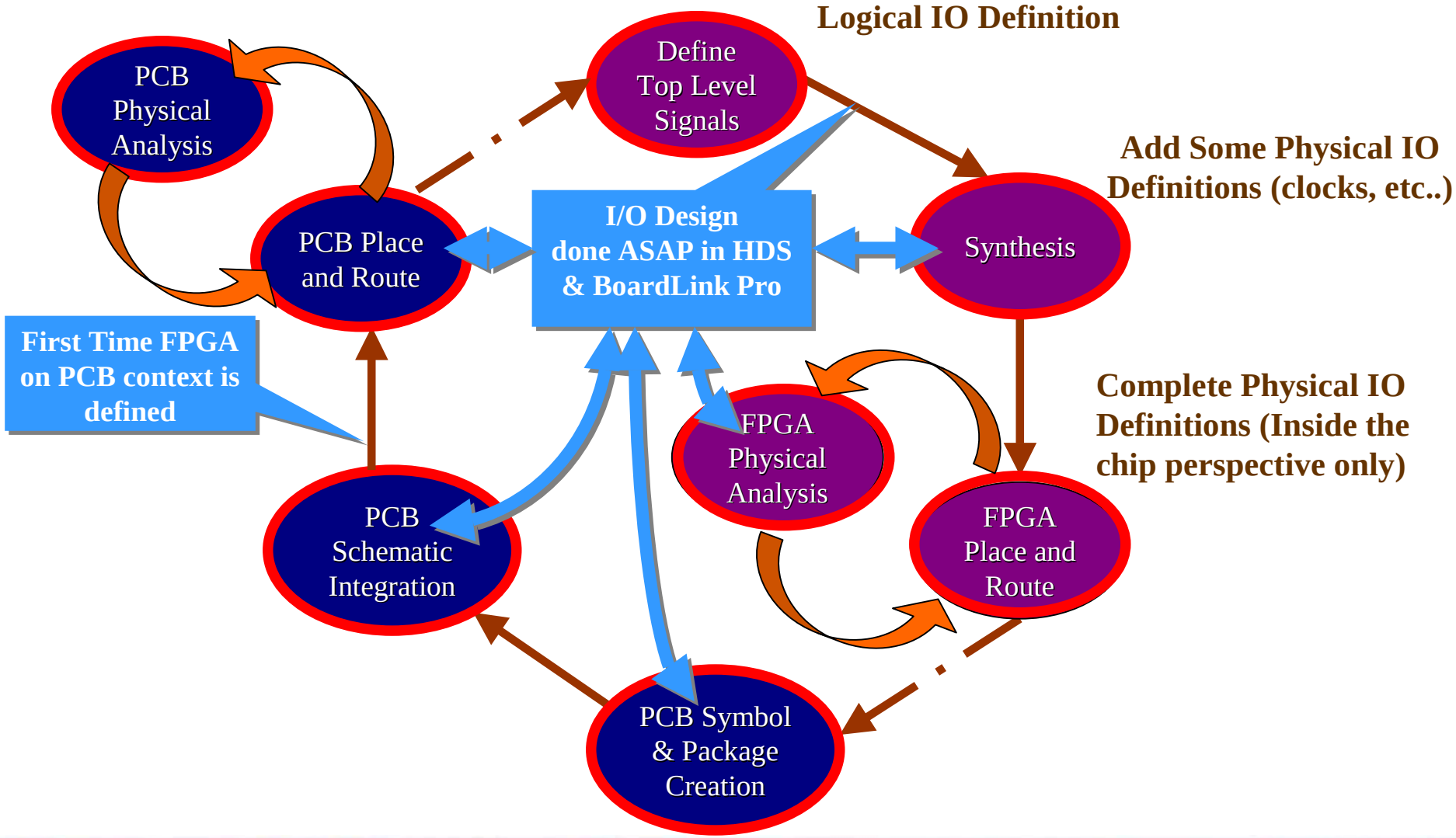
Platform Studio Integration

- **Supports MicroBlaze 2.00.a/2.10.a & PowerPC ppc405 2.00.c via Xilinx EDK 6.1i/6.2i Platform Studio**
- **Xilinx 6.1i/6.2i (ISE Foundation)**
  - **Integrated P&R**
- **HDS Browser Simulation view for Model*Sim***
- **Side Data Synthesis view for: LeonardoSpectrum, Precision Xilinx XST Syn*plify***



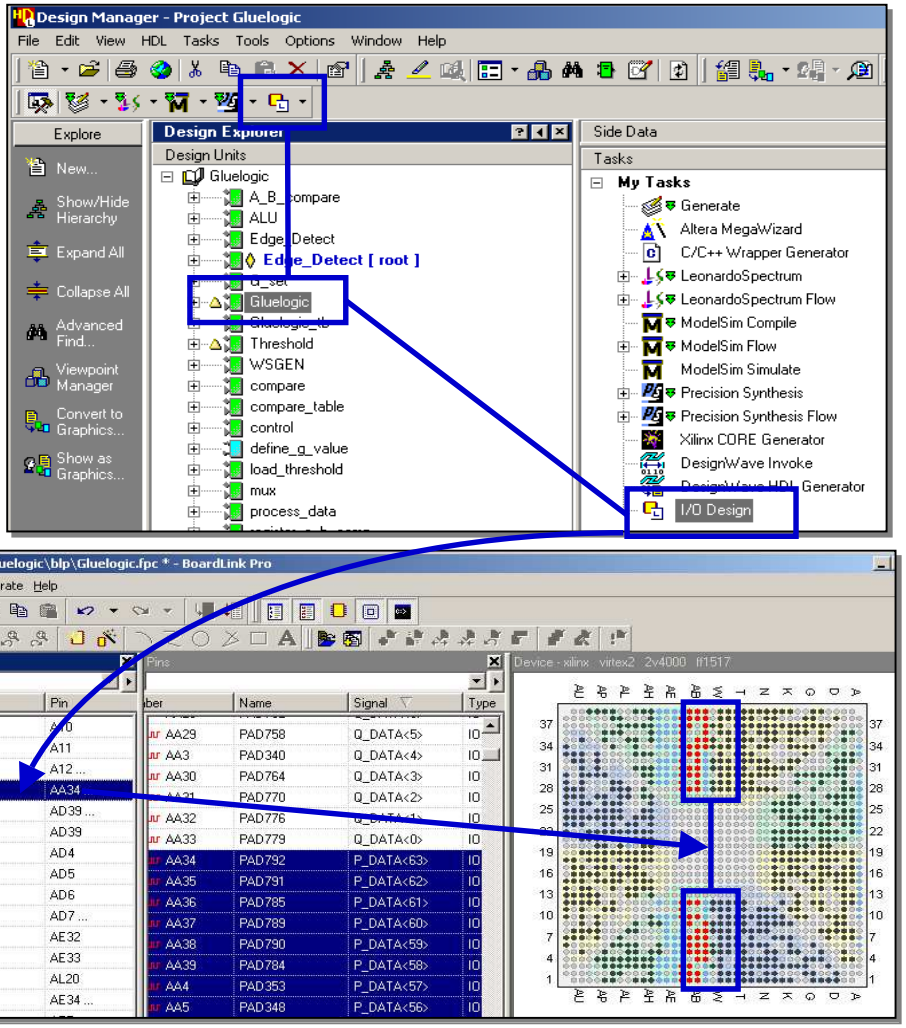


FPGA/PCB Integration



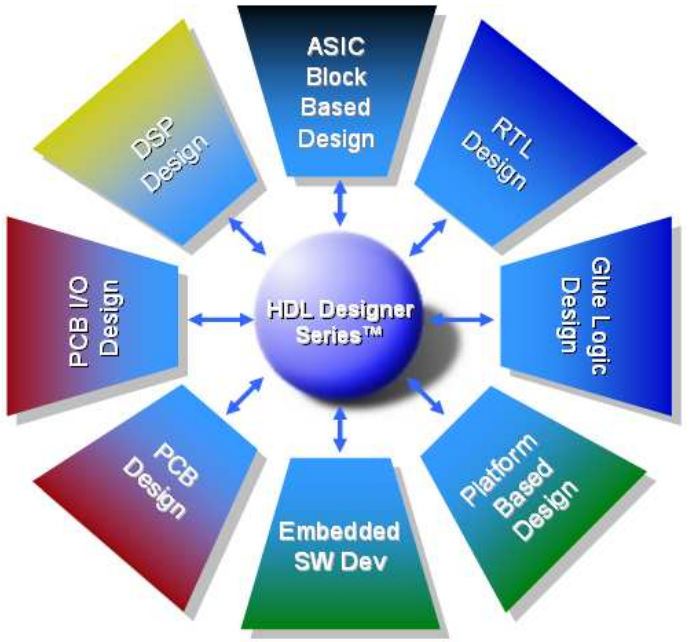
FPGA/PCB Integration

- **FPGA / PCB Integration Management**
  - **Board Station, Expedition, PADS**
  - **Intelligent targeting of Vendor, Device & Package**
  - **Drag & drop Pin & I/O Standard assignment**
  - **Creates and fractures Symbols**
  - **Creates & updates Schematic connectivity**
  - **Creates & maintains constraint files**
    - **Precision, LeonardoSpectrum, Syn*plify*, Synopsys**



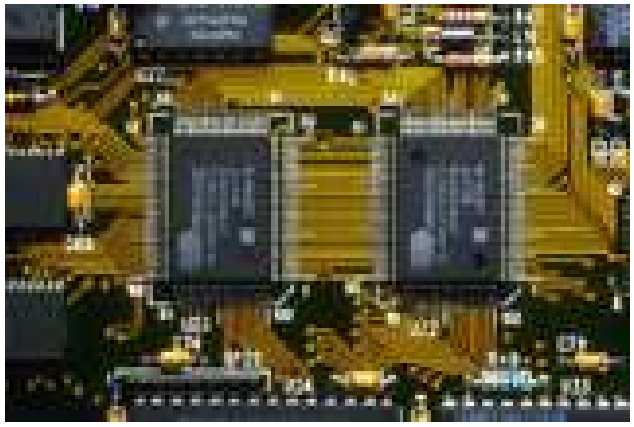
Designing Platform FPGAs

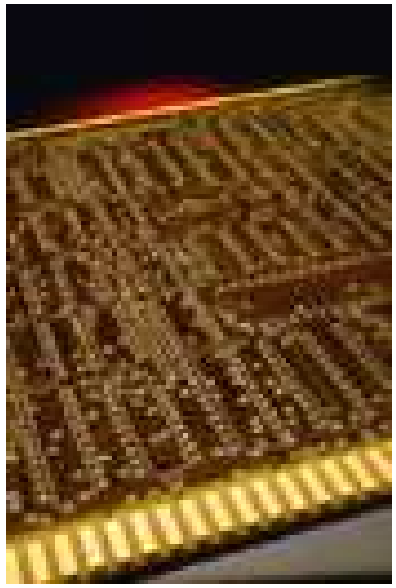
- **Optimizing Platform Performance**
- **Rapid Platform Prototyping**
- **Platform Design Verification**
- **Platform Example**

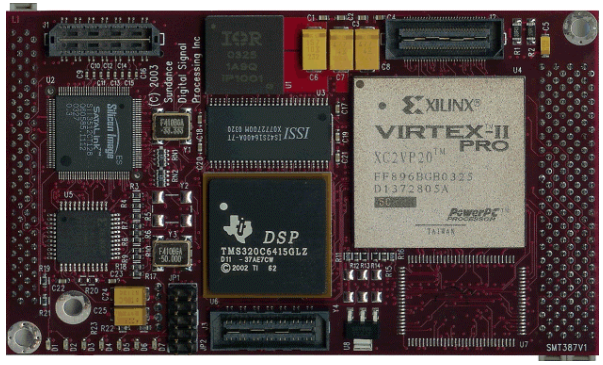


Rapid Platform Prototyping

- **Development Boards and PCB Design**
- **Verification**



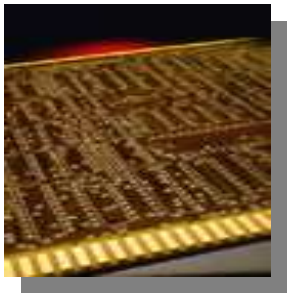


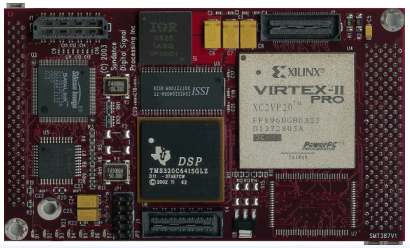


ModelSim

Development Boards and PCB Design

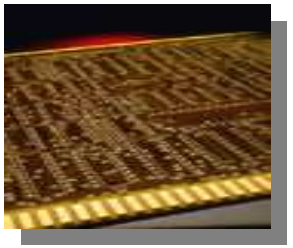
- **Effective use of development boards and development of the PCB in parallel can greatly increase productivity**
  - **Concurrent logic development**
  - **Concurrent SW development**
    - **Instantly download and test SW and/or logic in the development board**
- **But, poses challenges…**
  - **Managing the pin-out changes from the design as targeted to the development board and the PCB**
    - **Changing I/O changes the P&R therefore performance of the platform!**

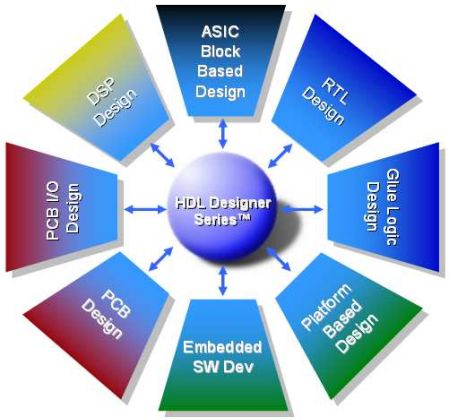


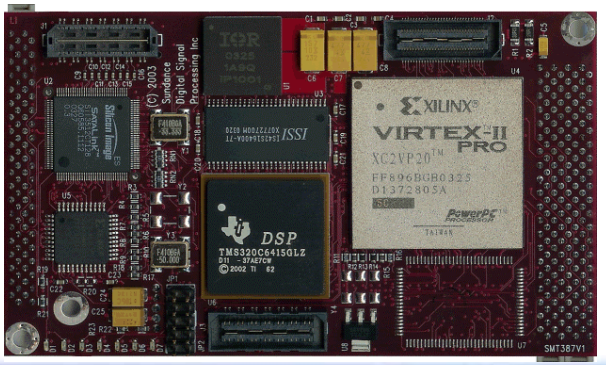


HDS + BoardLink Pro+ Precision Physical

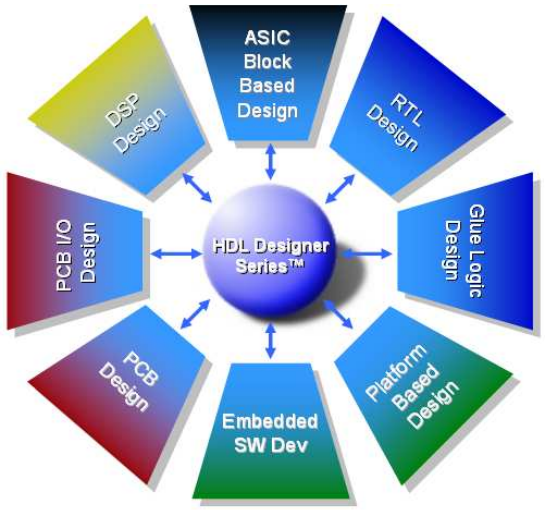
- **HDS - Manages the platform design and integrates with:**
  - **BoardLink Pro™ to easily move between the development board and PCB design**
    - **Swap pins to enabled better routability and signal integrity**
    - **Automatically synchronize HDL design and PCB design (symbols, pin outs, etc)**
  - **Physical™ to adjust to the changes in physical placement of the I/Os to maintain platform performance**

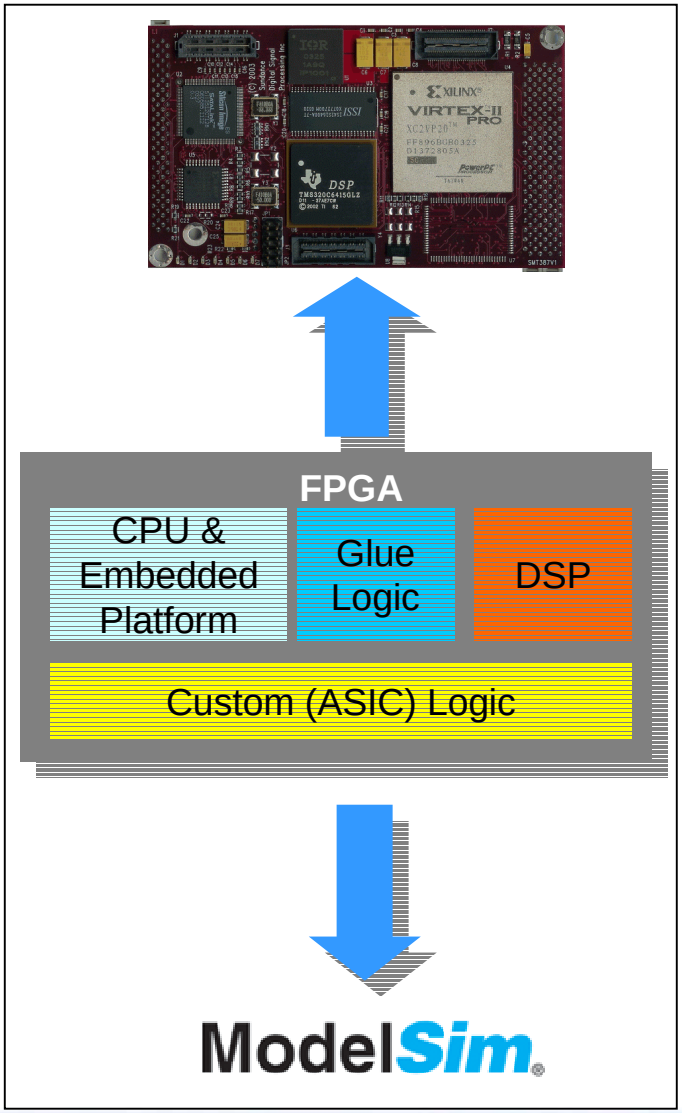






Verification

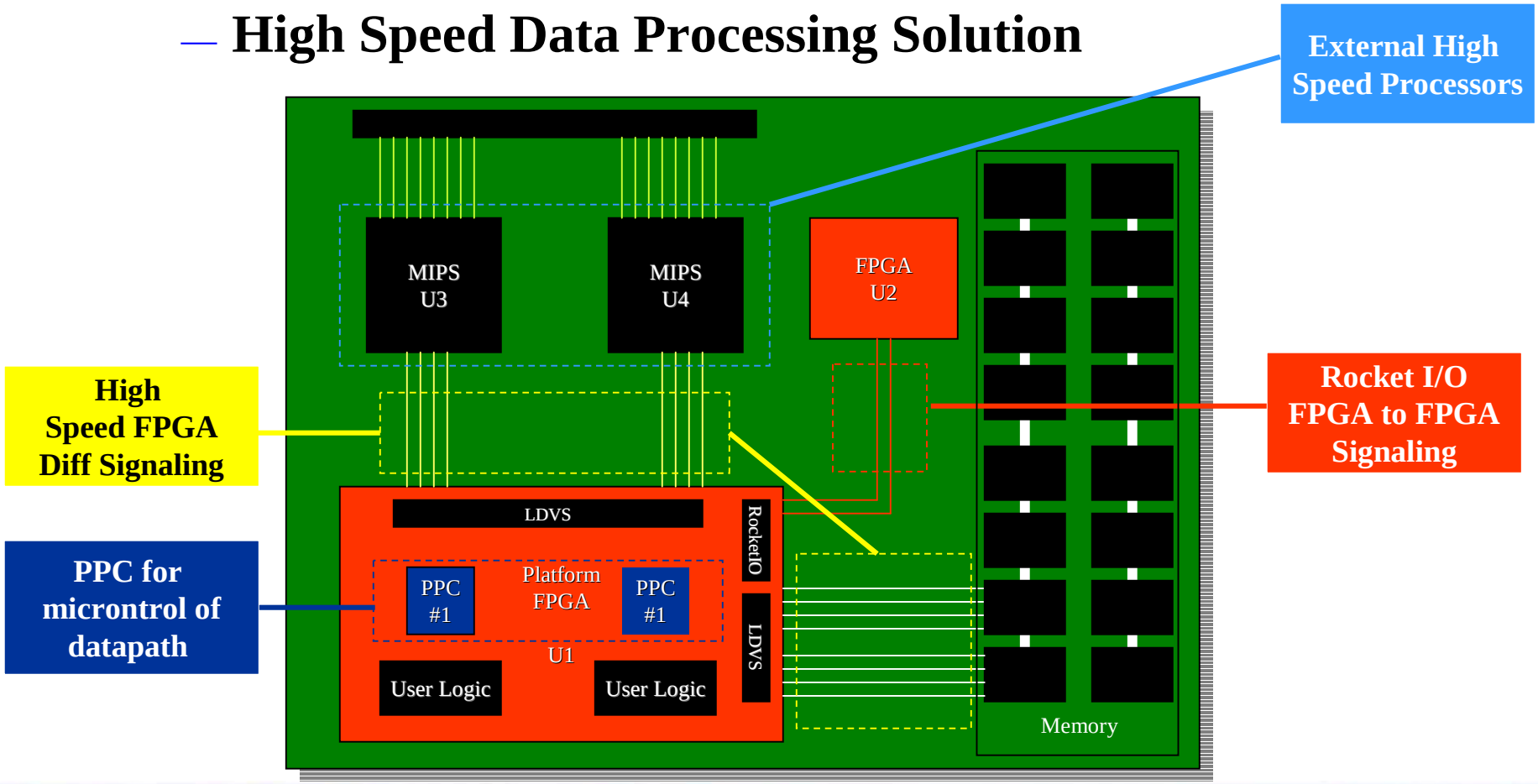




- **HDS can manage the verification of the platform design to the:**
  - **Development board for fast real time testing with software**
  - **Simulator environment for stand alone IP development**

Platform Example

- Let's look at a typical example design
  - High Speed Data Processing Solution



Integrated System Design

- **Applying Integrated System Design techniques to this design example merges:**
  - **System Design**
  - **High Speed PCB I/O Design**
  - **High Speed PCB Physical Design**
  - **Embedded processors (Nios,Microblaze,PPC405,ARM)**
  - **High Data Rate Memory FPGA Interface**
  - **High Data Rate External Processor Interface**
  - **High Data Rate FPGA to FPGA Interface**
  - **FPGA DSP development**
  - **User logic development**
  - **SW Development**

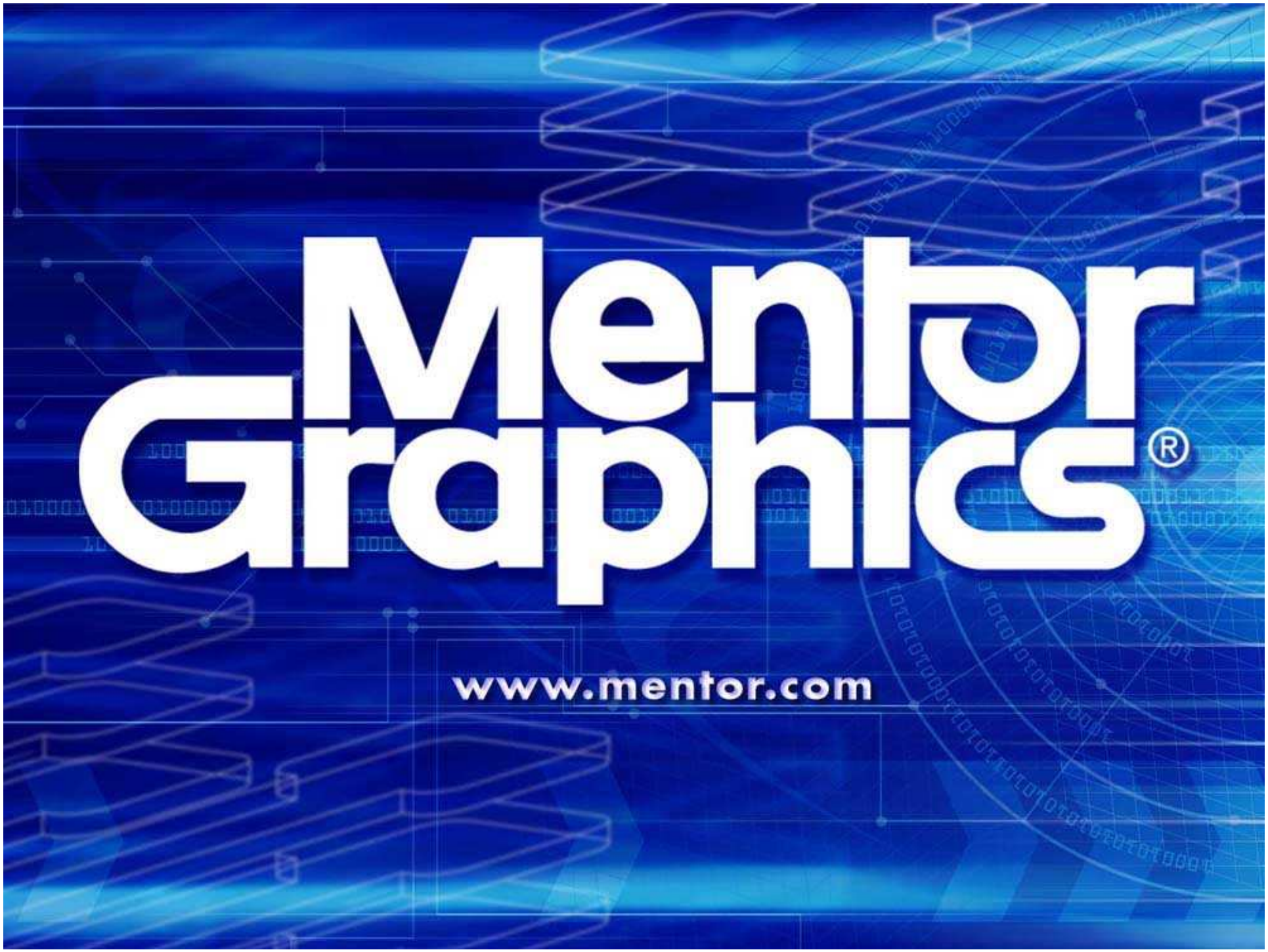
ISD
Integrated System Design

System on Chip

System on Board

Summary

- **Platform FPGA Designs are Growing Quickly**
- **Effectively Utilizing Platform FPGA Across Disciplines for Optimal Performance On Chip and On Board Requires a Integrated System Design Methodologies/Solutions**
- **Harness the Power of Platform FPGAs with HDL Designer Series**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