

Lecture Notes

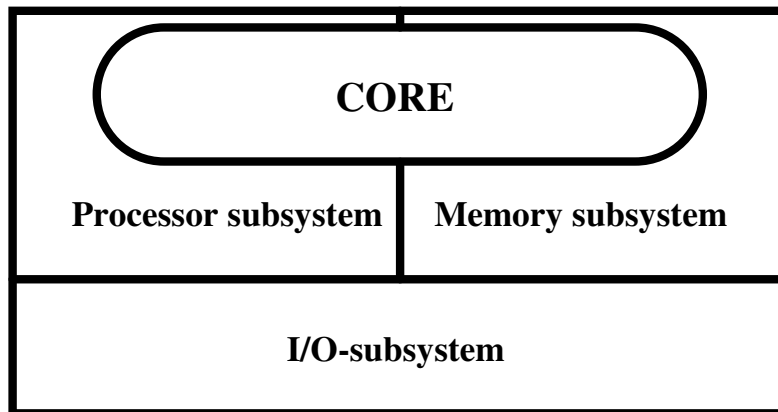
IAF0042

Arvo Toomsalu

Computer Architecture

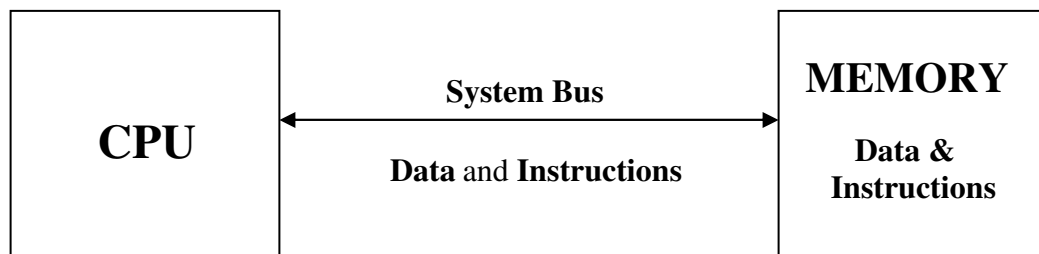
Introduction

Computer Model

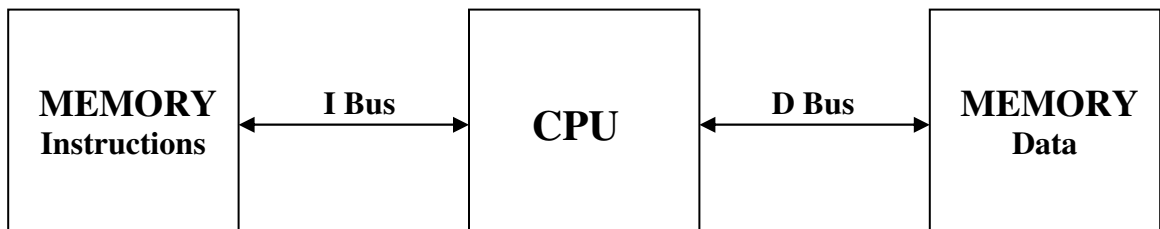


Classical Architectures

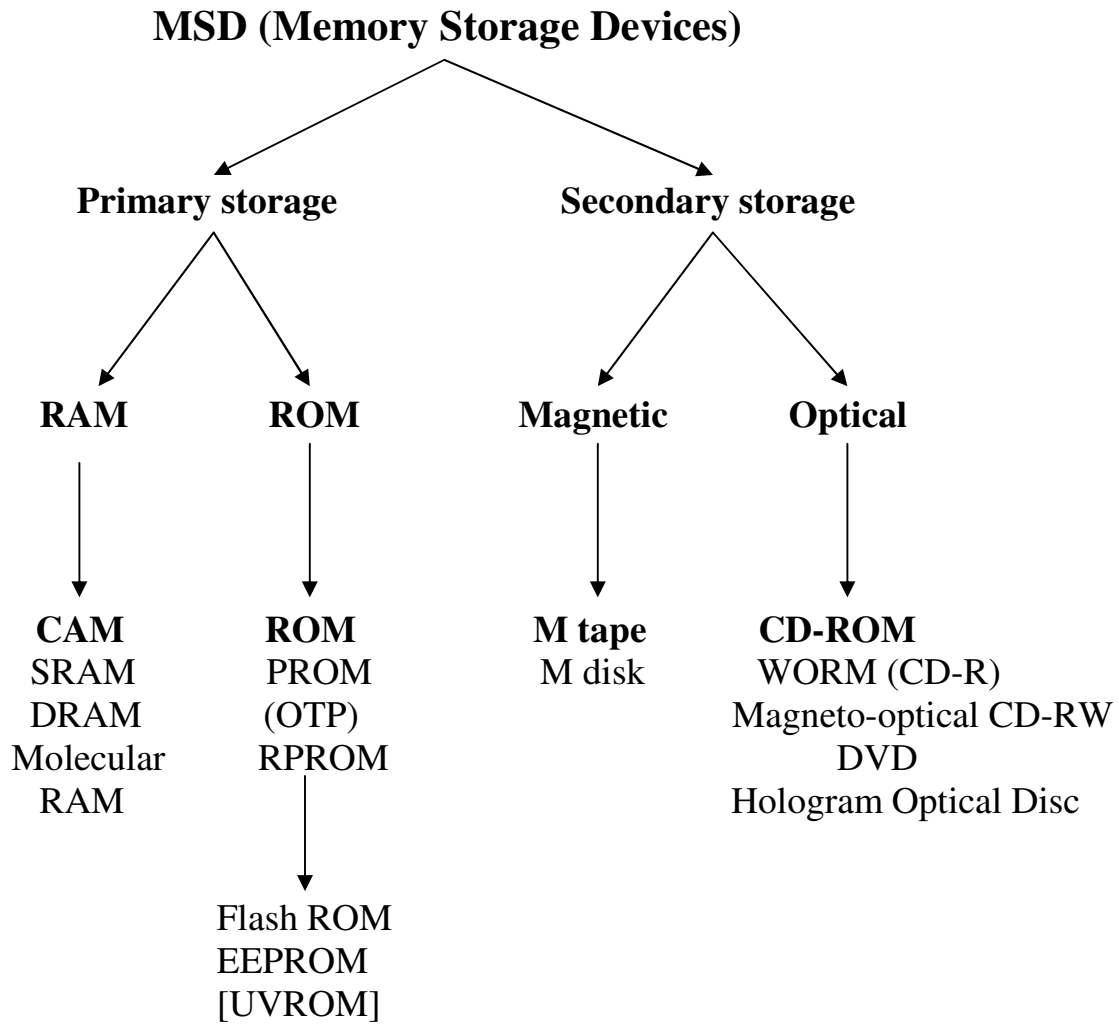
Princeton or von Neumann architecture



Harvard architecture

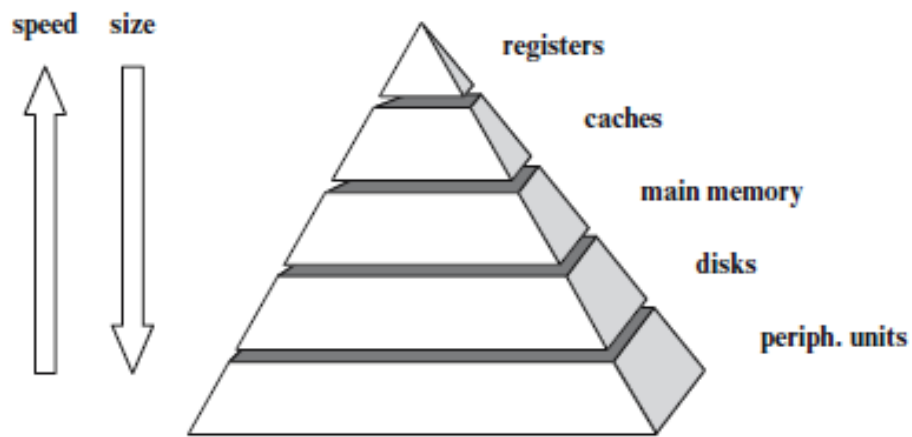


MEMORY SYSTEM



CAM – Content Addressable Memory (Associative Memory)

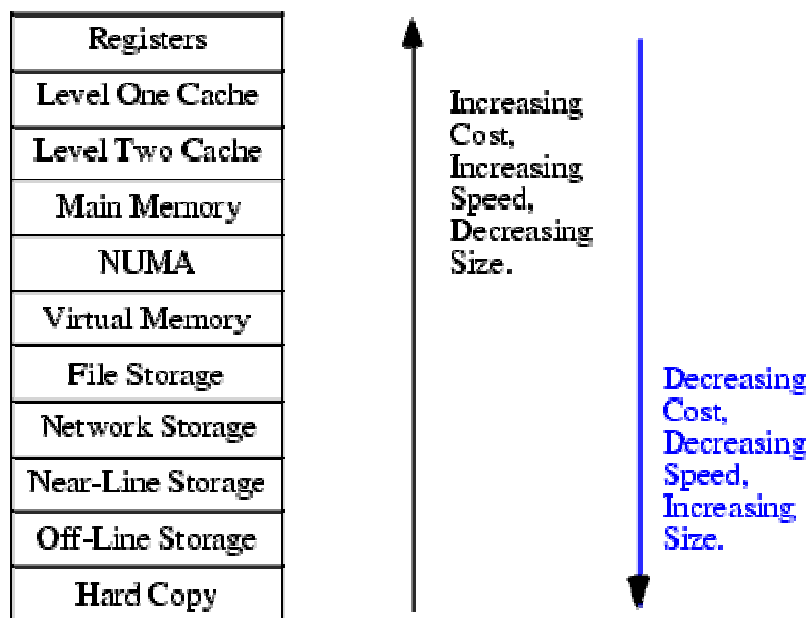
Memory Hierarchy



Memory hierarchy wide-spread model

A typical hierarchy consists of:

1. Register file;
2. Per-processor level 1 (L1) instruction and data cache;
3. On-chip, shared unified level 2 (L2) cache;
4. Off-chip level 3 (L3) cache;
5. Main memory;
6. Hard disc for virtual memory.



Extended memory hierarchy model

Memories Internal (architectural) Organization

DRAM – dynamic RAM

SDRAM - synchronous dynamic RAM

DDR-SDRAM - double-data-rate SDRAM

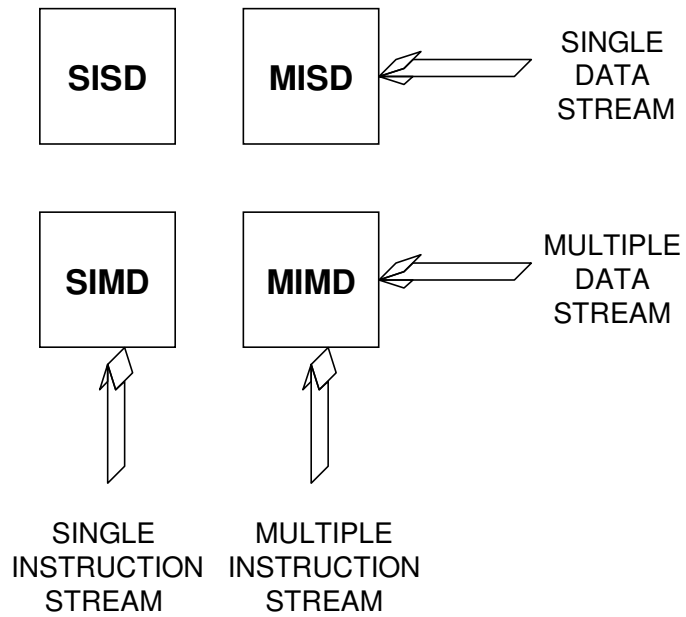
MDRAM – multi-bank DRAM

ESDRAM - cache-enhanced DRAM

etc.

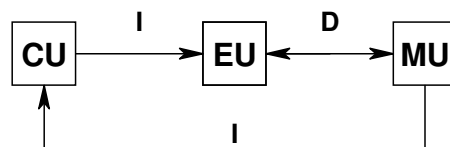
MULTIPROCESSOR SYSTEMS

Flynn-Johnson taxonomy

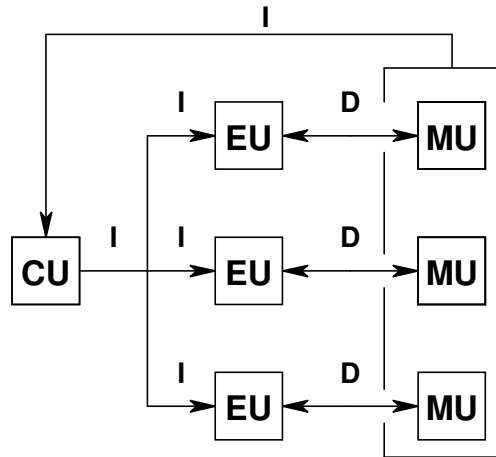


SISD Architecture

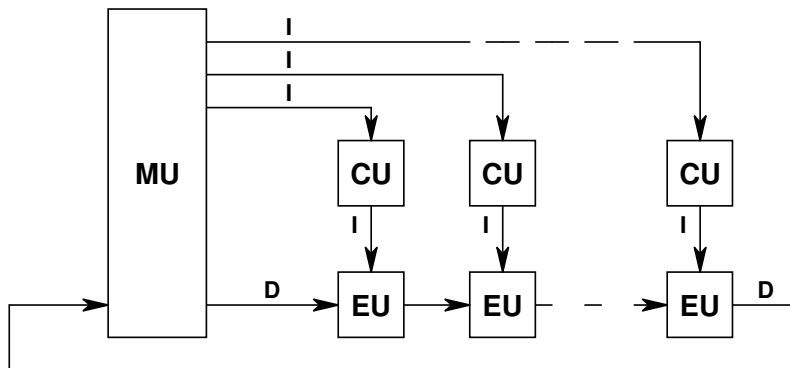
I- instructions; D – data



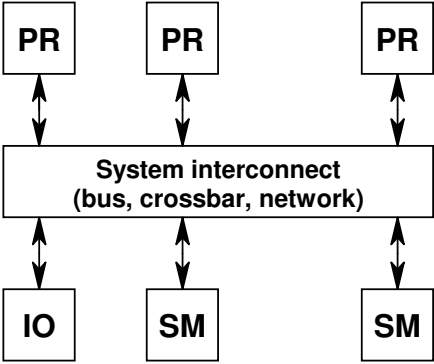
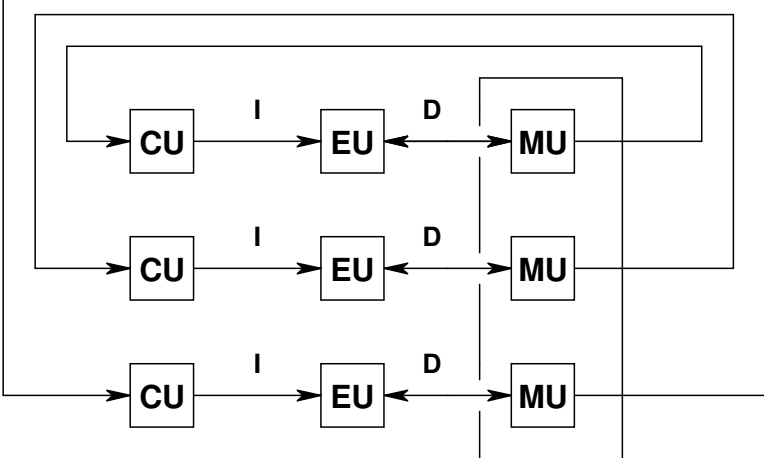
SIMD Architecture



MISD Architecture

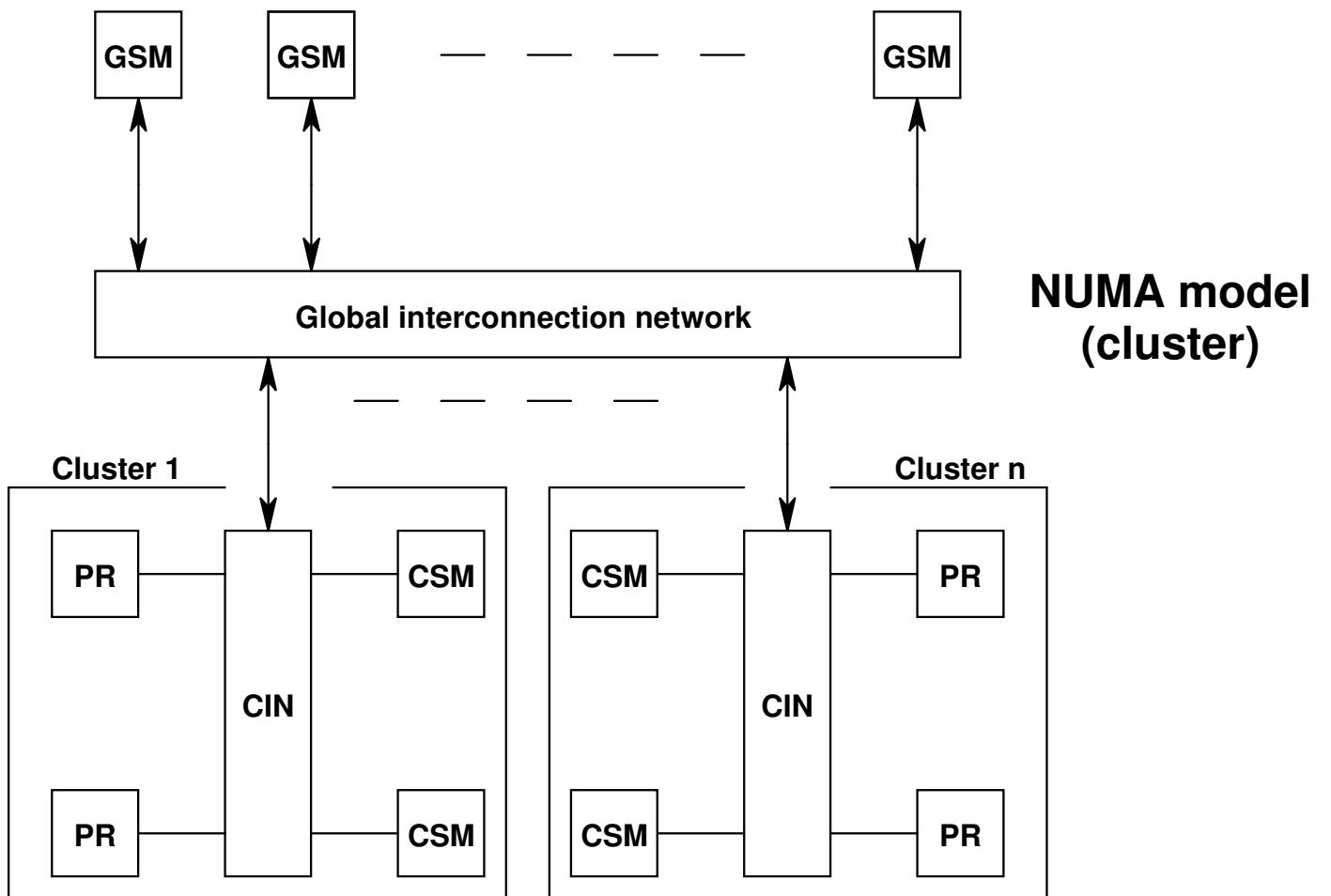


MIMD Architecture



UMA model

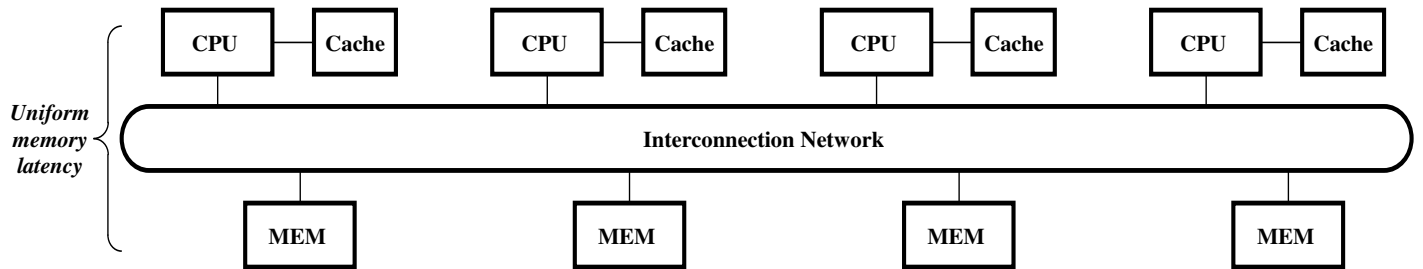
SM - Shared Memory
 LM - Local Memory



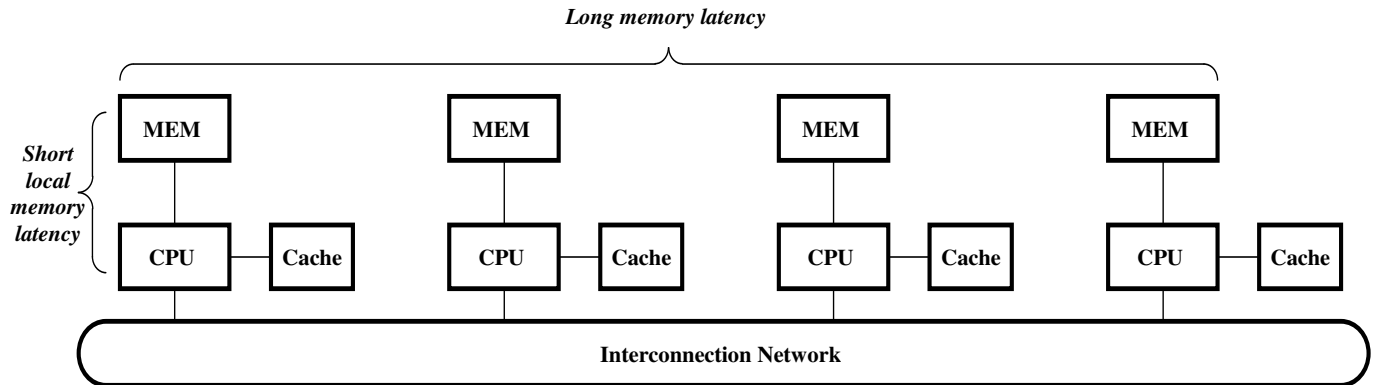
PR – processor; **IO** – input-output unit; **SM** – shared memory; **LM** – local memory;
GSM – global shared memory; **CSM** – cluster shared memory;
CIN – cluster interconnection network.

UMA versus NUMA

UMA



NUMA



Microprocessor systems capabilities are related to system processing capabilities include:

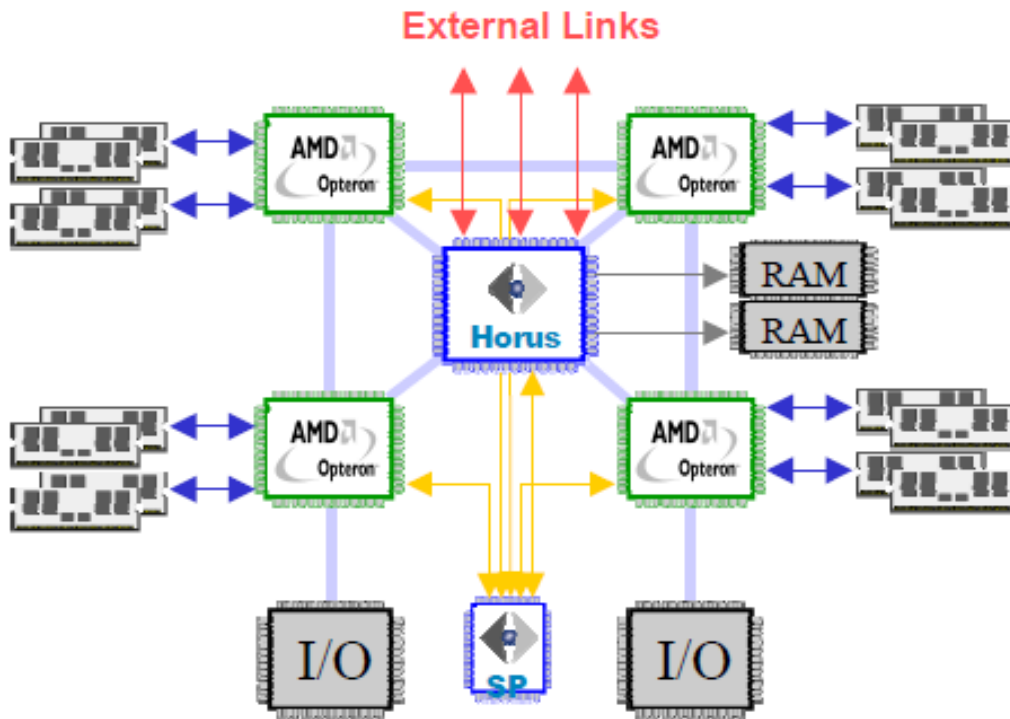
Cost-performance

Throughput (operations per time unit)

Resource sharing

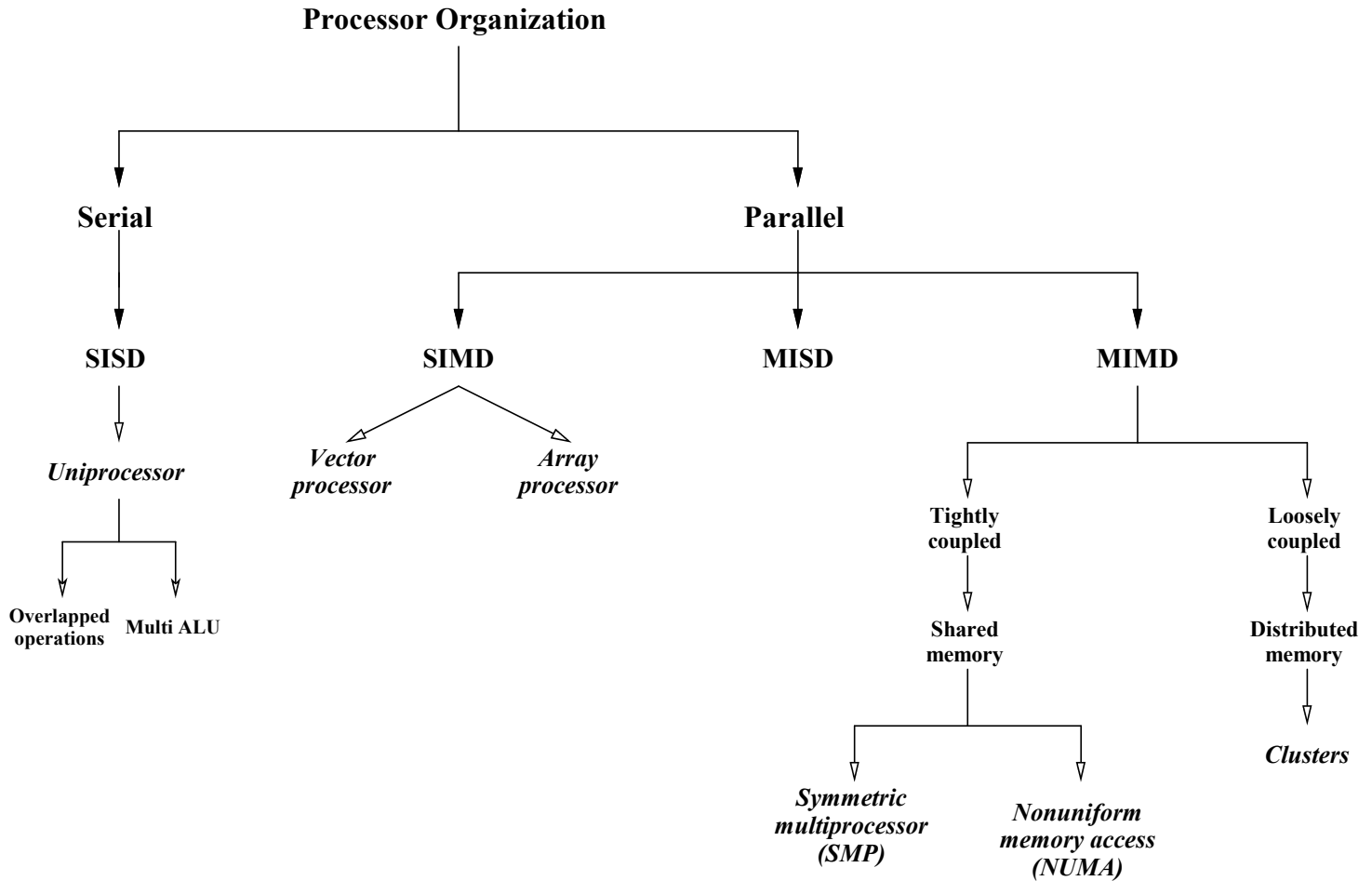
Example

The Newisys ASIC implementation *HORUS*



Summary

Taxonomy of Mono- and Multiprocessor Organizations



Literature

Arthur W. Burks, Herman H. Goldstine, John von Neumann. Preliminary Discussion of the Logical Design of an Electronic Computing Instrument.

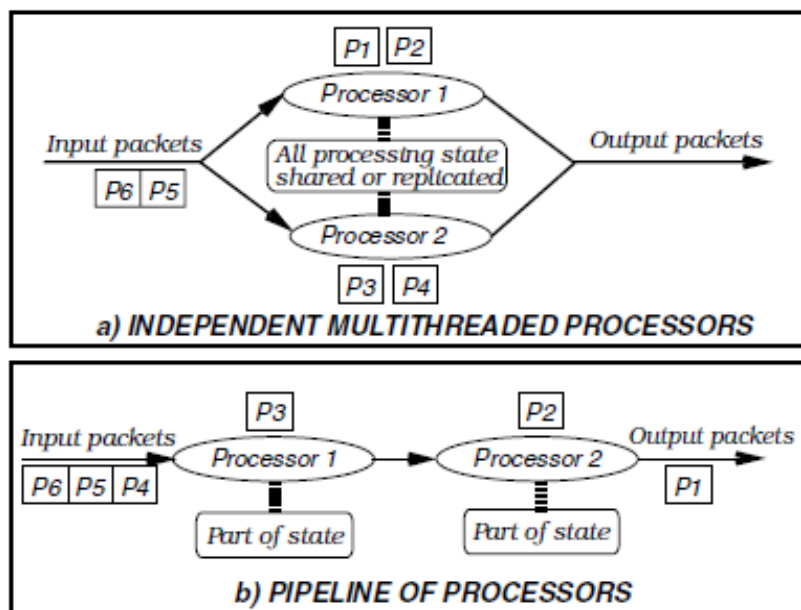
Arvutivõrgus: <http://www.cs.unc.edu/~adyilie/comp265/vonNeumann.html>

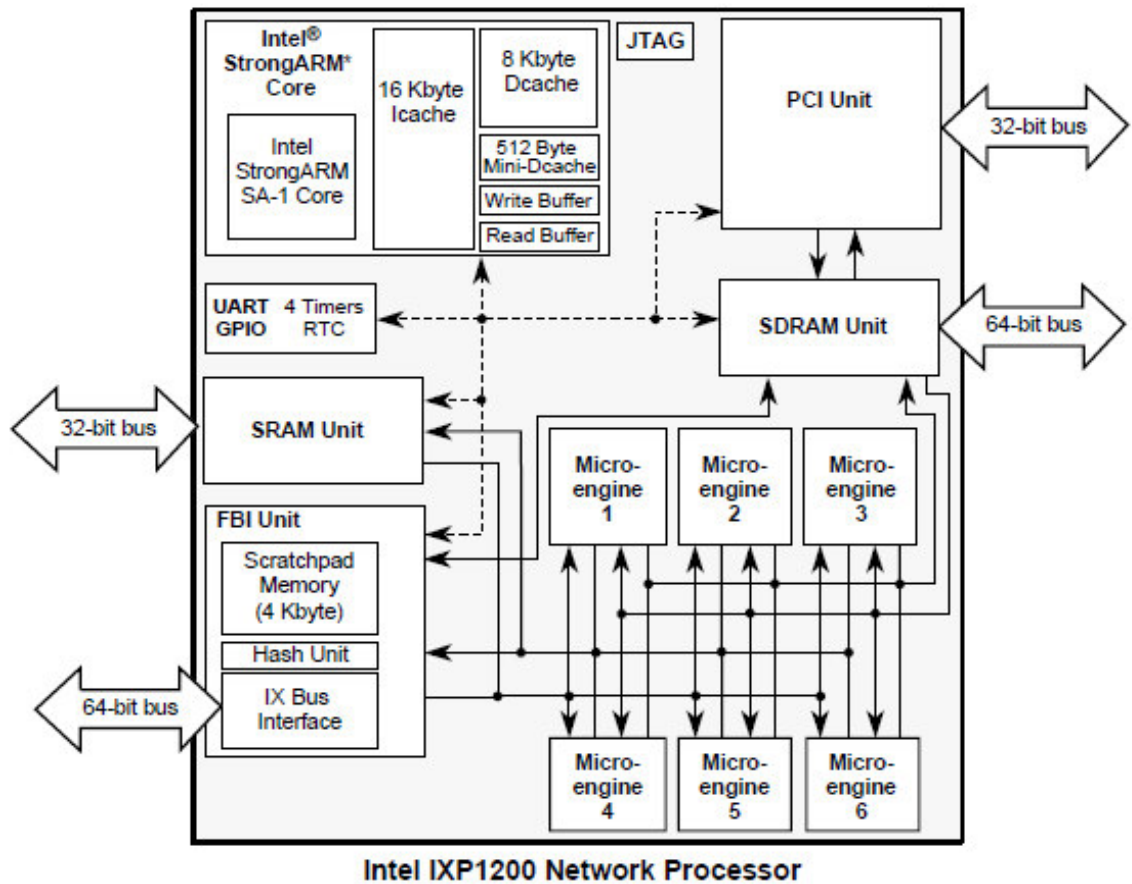
Network Processors

Network processor is a programmable CPU chip that is optimized for networking and communications functions.

Two common approaches (**a, b**) to **parallelism in network processors**:

- a.** Input packets are distributed among multiple processing units to divide the load.
- b.** Input packets flow through a pipeline of processing elements.





Notes:

- * Other brands and names are the property of their respective owners.
- 32-bit Data Bus
- 32-bit ARM System Bus

Graphics Processor

A **graphics processor** (video card, graphic accelerator card, display adapter) is a **special purpose microprocessor** specifically designed to generate signals to drive a video monitor.

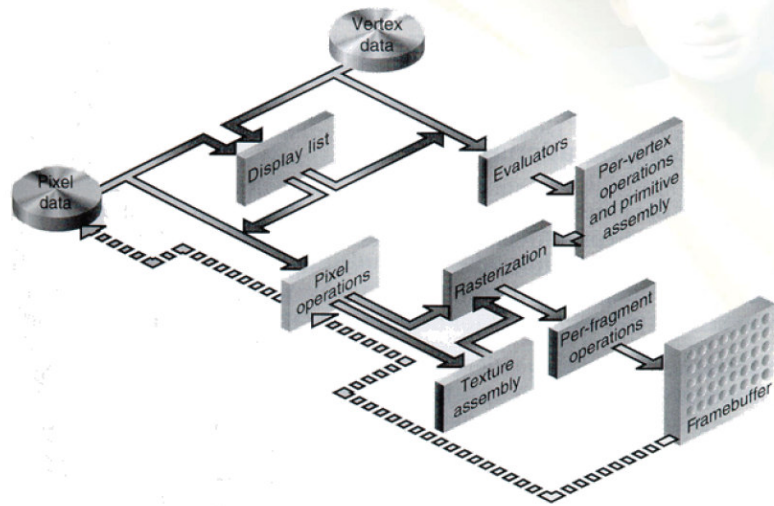
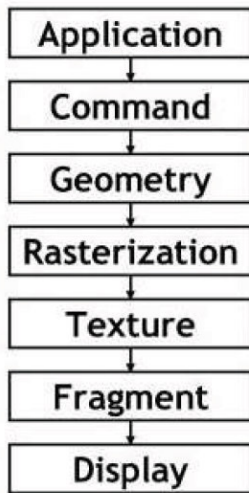
In graphics applications, complex shapes and structures are formed through the sampling, interconnection and rendering of more **simple objects (primitives)**.

Graphics primitives may include lines, characters, areas (triangles and ellipses), and shapes (polygons, spheres, cylinders and the like).

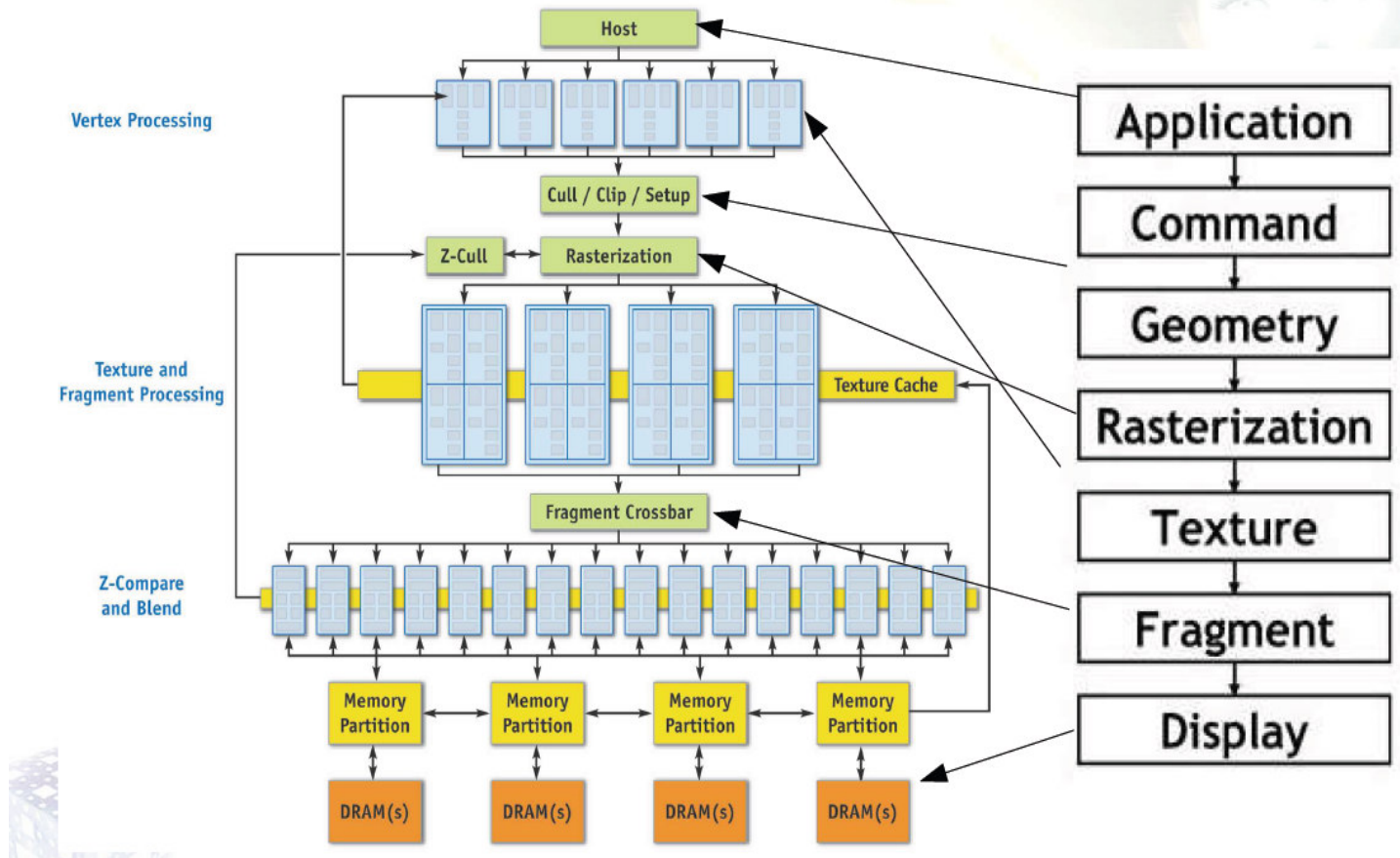
These **primitives** are formed by the interconnection of individual pixels.
3D graphics images, there are three dimensions, include the dimension of depth (Z dimension).

Modern computers typically produce graphical output using a sequence of tasks known as a **graphics pipeline**.

The Graphics pipeline



NVIDIA GeForce 6800 Block Diagram

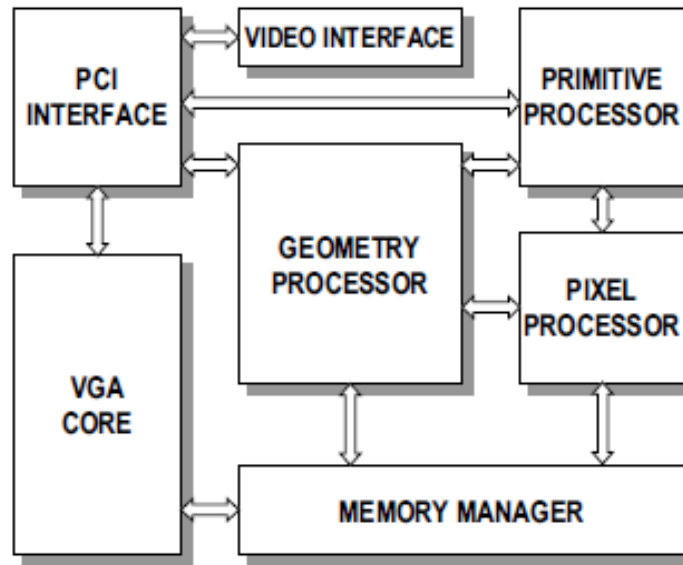


NVIDIA GeForce 6800 Features

1. High performance;
2. Multiple small independent memory partitions for improved latency
3. Early culling and clipping, cull non-visible primitives at high rate;
4. Rasterization supports aliased and anti-aliasing and triangles, etc;
5. Z-Cull, allows high-speed removal of hidden surfaces;
6. Occlusion Query, keeps a record of the number of fragments passing or failing the depth test and reports it to the CPU.

Pyramid3D Real-time Graphics Processor
TriTech Microelectronics, Inc.

Pyramid3D System Architecture



Multiprocessor architecture

Single-chip 3D graphics solution, which consists of:

- **Geometry Processor**
- **Primitive Processor**
- **Pixel Processor**

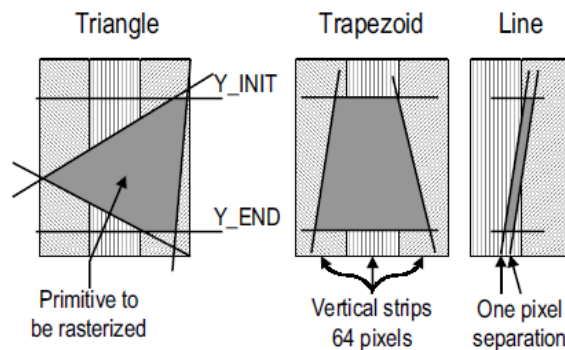
Geometry Processor

- 3-issue VLIW architecture
- 32-bit fixed point vector datapath
 - Block floating point support
- Hardware division unit
- Integrated data memory
 - 3 × 128 words 2-port SRAM
- Instruction cache
 - 4-way set associative
 - 4 × 128 word blocks

Primitive Processor Features

- Hardwired unit
 - Fixed operations on user data
- Two FIFO's for load balancing
 - Each FIFO 64 130-bit words
- Primitives defined by 3 edge functions

Supported Graphics Primitives



Multimedia Processors

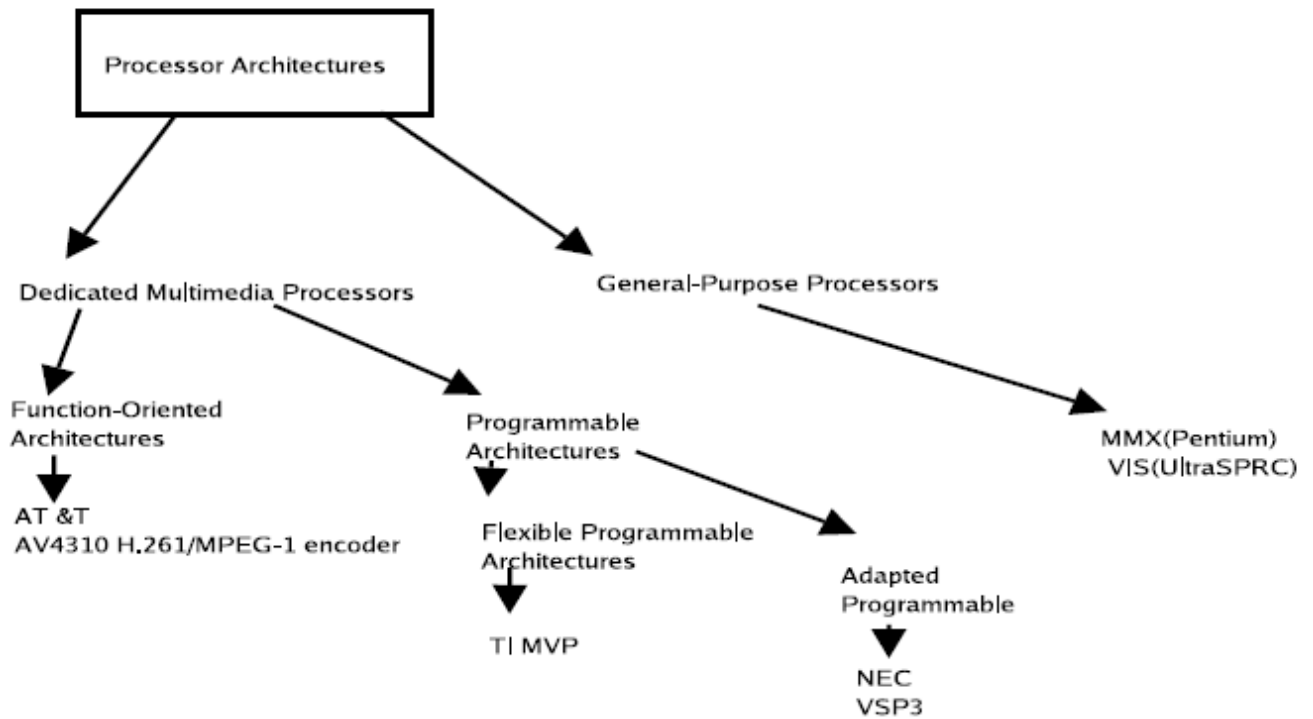
Multimedia is media and content that uses a combination of different content forms. **Multimedia** is integration of multiple forms of media: text, graphics, audio, video, communication etc.

Multimedia Applications Characteristics

The most important ones are:

- **Real-time response.**
- **Processing of streaming data.**
- **Significant fine and coarse grained data parallelism.**
- **Data reorganization.**
- **Small loops.**
- **High memory bandwidth requirement.**
The applications process large data sets, putting a severe burden on memory system.
- **Small data types.**
- **MMAs perform significantly more arithmetic operations than GPAs.**
-

Classification of Processor Architectures that Support Multimedia



Dedicated multimedia processors

The dedicated processors are typically custom designed architectures intended to perform specific multimedia functions. Some advanced multimedia processors provide also support for 2D and 3D graphics applications.

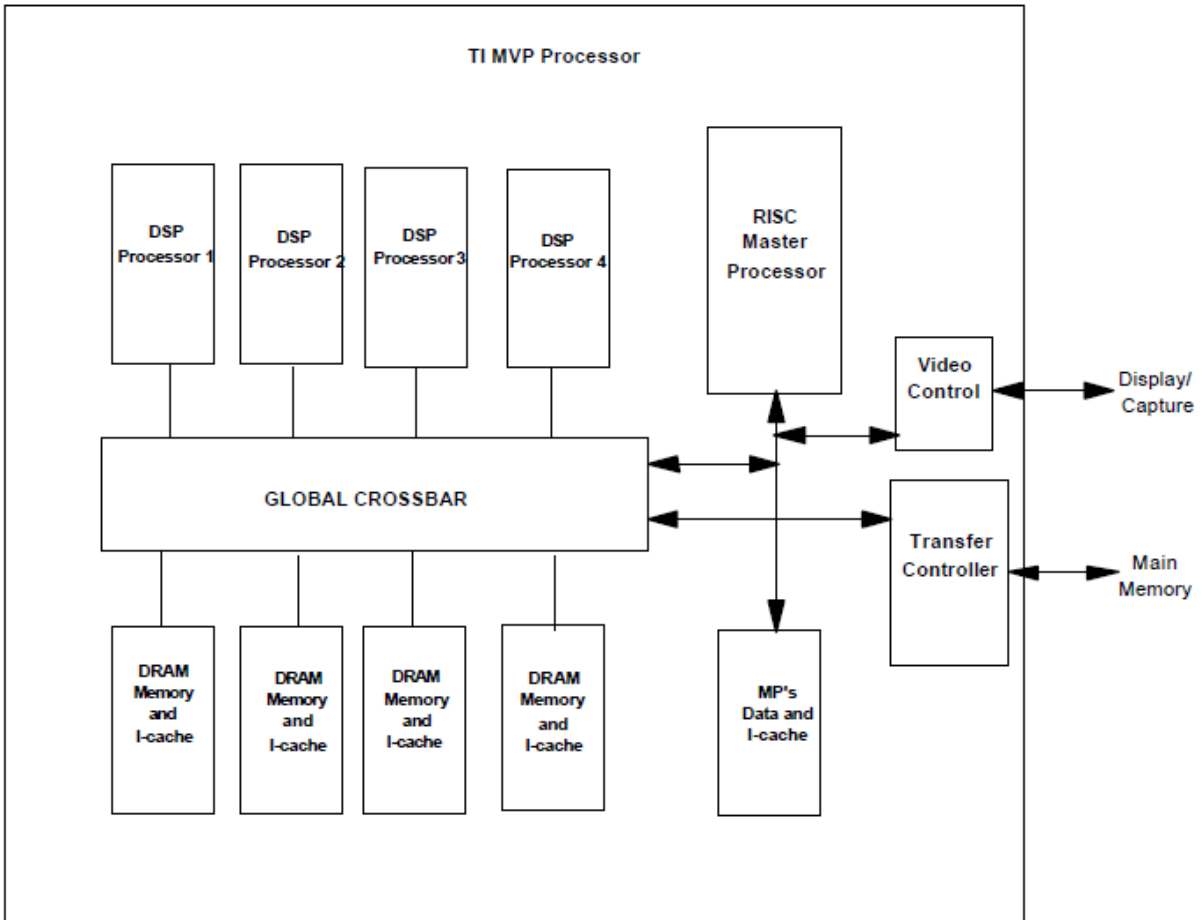
Designs of dedicated multimedia processors ranges from fully custom architectures, referred to as function specific architectures, with minimal programmability, to fully programmable architectures.

A. Function specific architectures

Function specific dedicated multimedia architectures provide limited, programmability, because they use dedicated architectures for a specific encoding or decoding standard.

B1. Flexible programmable architectures

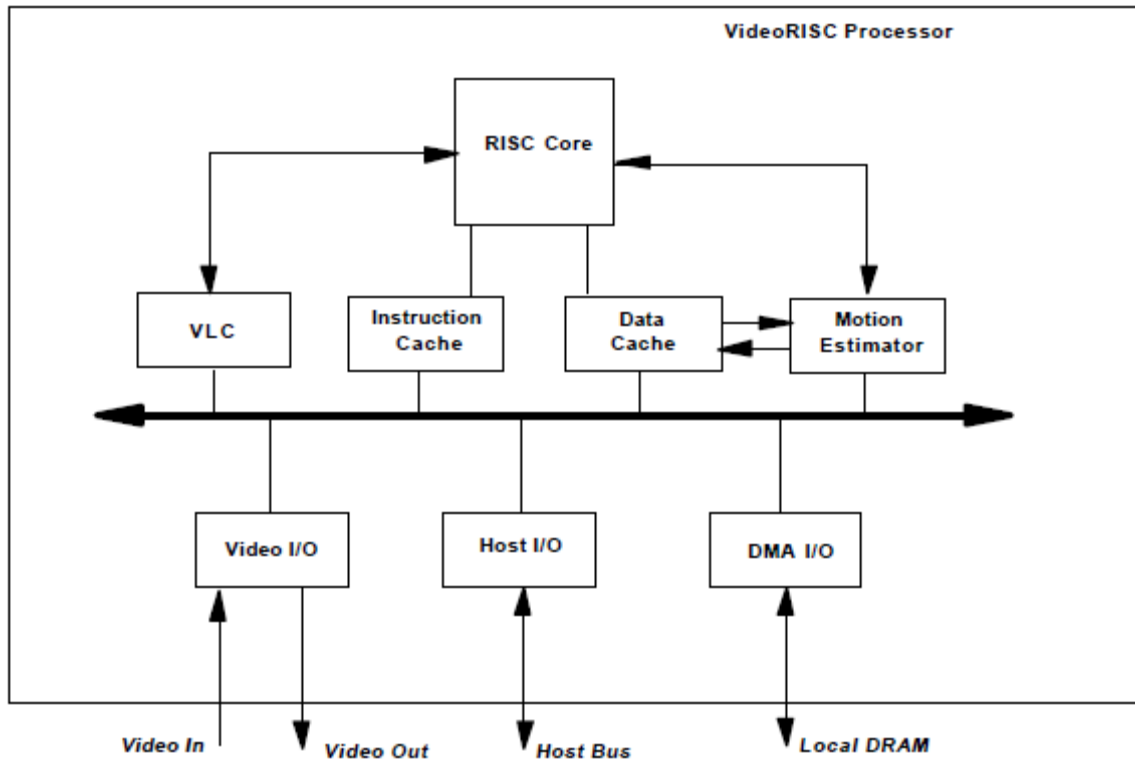
These processors can have a moderate to high flexibility, are based on **coprocessor concept** as well as **parallel datapaths** and **deeply pipelined designs**.



TI's Multimedia Video Processor

B2. Adapted programmable architectures

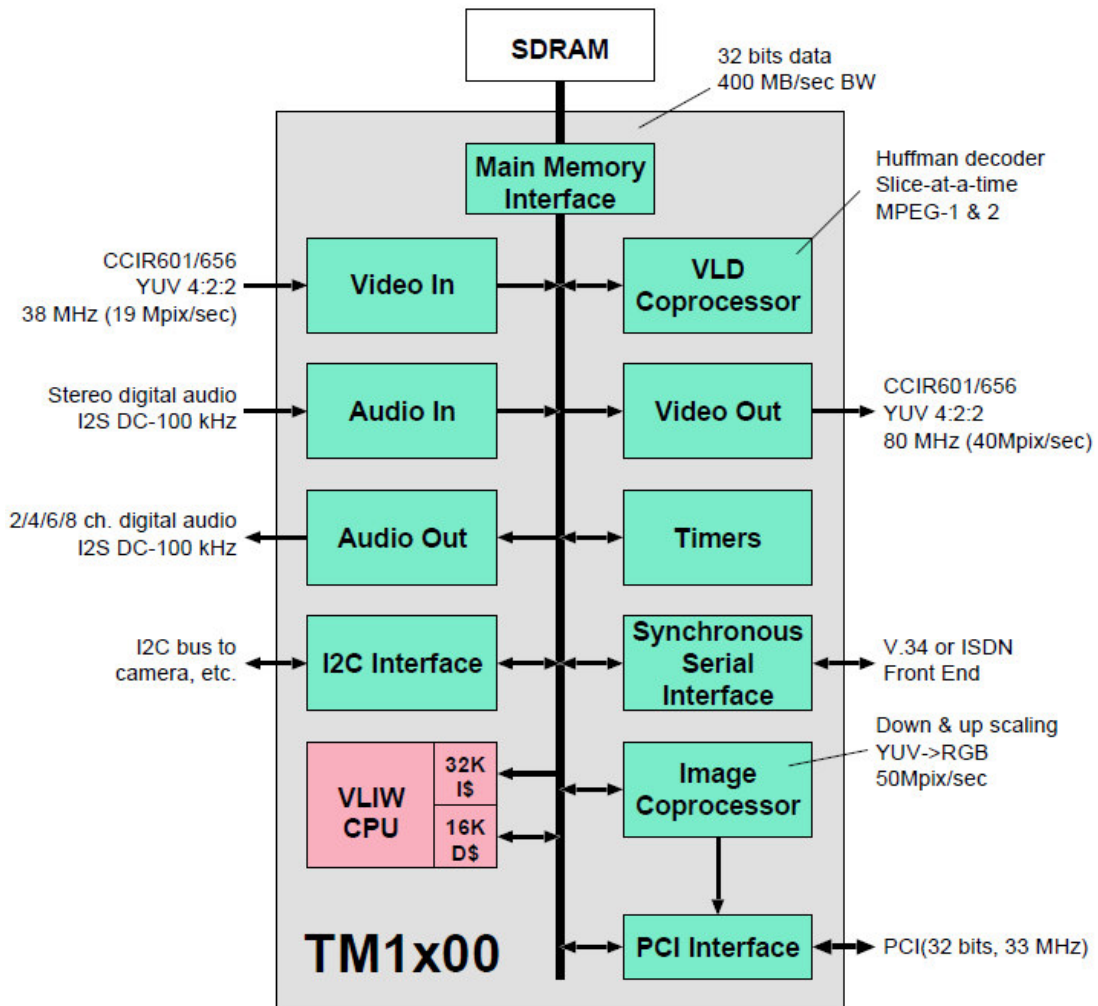
These processors provide increased efficiency by adapting the architecture to the specific requirements of video coding applications.

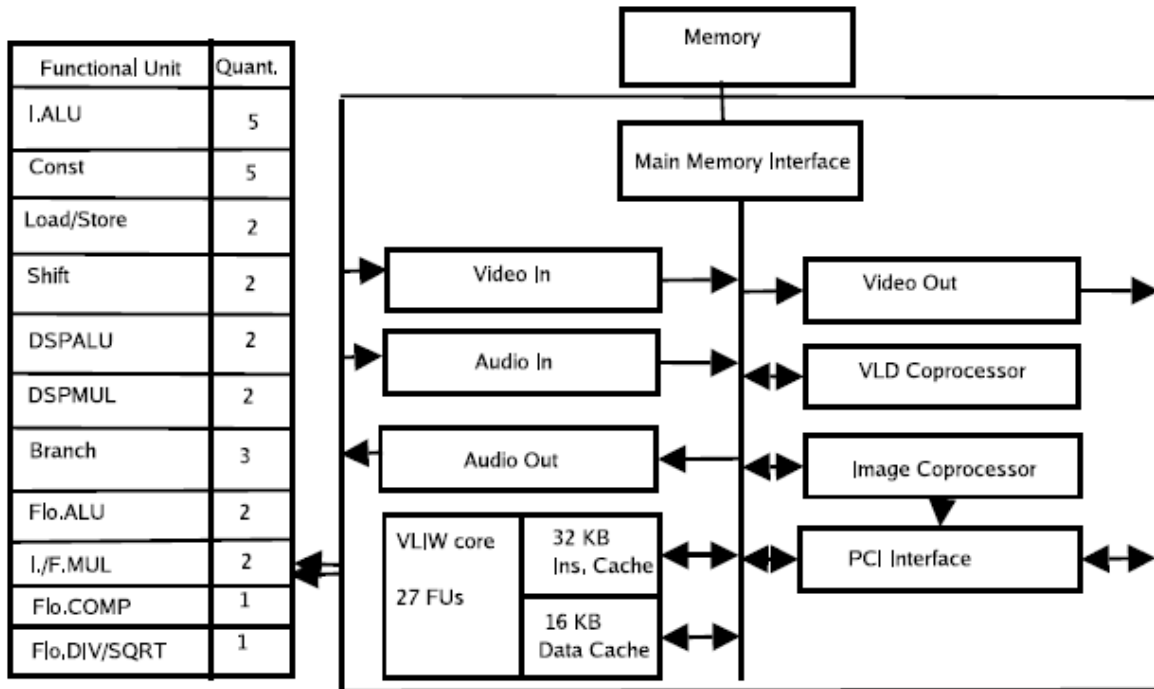


C-Cube's VideoRISC processor

The **modern advanced dedicated multimedia processors** use **SIMD** and **VLIW** architectural schemes and their variations to achieve **very high parallelism**.

Philips TriMedia CPU64





Philips TriMedia CPU64 TM1x00 with VLIW-core

Processor's main characteristics are:

1. A 5-issue VLIW architecture with a 32-bit word size;
2. 27 functional units;
3. Any operation can be guarded to provide conditional execution without branching;
4. Instruction set and functional units optimized with respect to media processing;
5. A single multi-ported register file with bypass network, allowing 1-cycle latency operations;
6. 32 kB, 8-way instruction cache;
7. 16 kB, 8-way, quasi-dual ported, data cache;
8. A variable-length (compressed) instruction set design.

Example

ZMS-08 Media Processor **ZiiLABS Pte Ltd.**

Typical Application

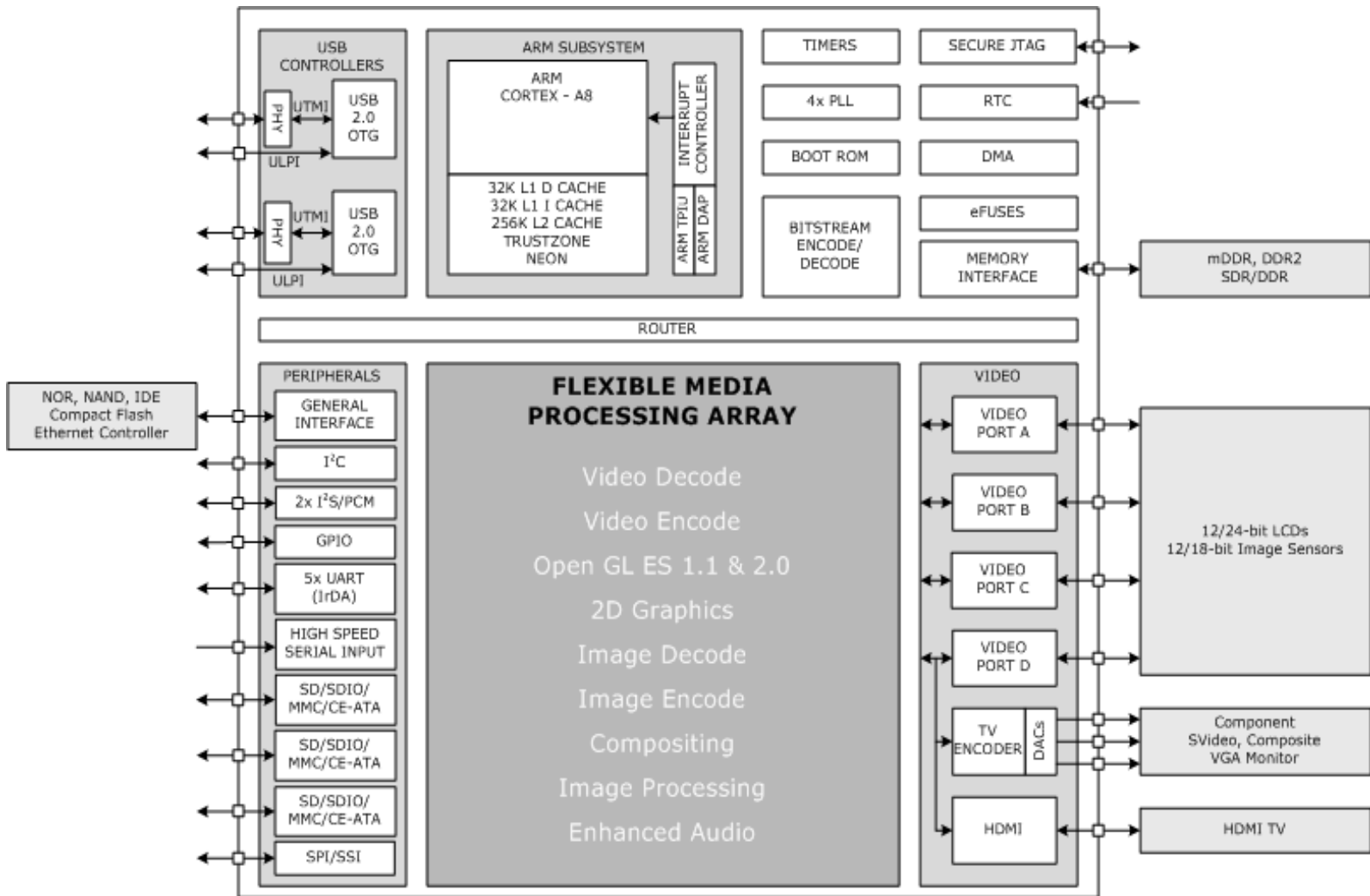
- Web tablets
- Netbooks
- Connected TVs
- Portable infotainment
- Digital media hubs
- Point of service terminals
- Video conferencing systems

Main Features

- Blue-ray Quality 1080p H.264 video decode
- 1080p H.264 video encode
- 720p H.264 video conferencing
- Multi format media codecs
- ARM Cortex-A8 at 1GHz
- Accelerated graphics and compositing
- Advanced image signal processing
- Rich peripheral integration and connectivity

Performance

- Blue-ray Quality 1080p H.264 video decode at 40mbps
- Simultaneous 720p H.264 video encode and decode
- 1080p H.264 video encode
- ARM Cortex-A8 at 1GHz



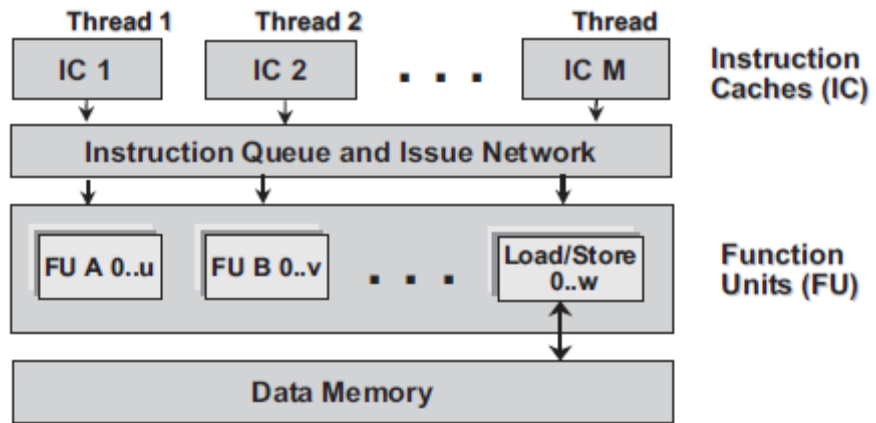
General-purpose (GP) processors

GP processors provide *support for multimedia by including multimedia instructions into the instruction set.*

Multimedia Processors Architecture Development Trends

There are three new architectural concepts:

1. **Reconfigurable computing;**
2. **Simultaneous multithreading (SMT):**



SMT based multimedia architecture

3. Associative controlling