High Level Synthesis for SoC design

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The tremendous achievements in the chip technology allow the production of chips with hundreds of millions of gates. At the same time, the design technology of such circuits only slightly improved in the last ten years, especially at the highest system level. The traditional digital system design flow contains the manual creation of system description at RTL with Verilog or VHDL code. As a result, the time-to-market is increased three to four times for such complex digital chips. The only possibility to reduce a gap between future technological capability and lagging designer productivity is to raise the design from the current RTL to the algorithmic or behaviour level and design new 4th generation HLS tools that can handle any types of digital systems.

At this meeting I will present Synthagate (former *Abelit*) which is the first true 4th generation High Level Synthesis (HLS) tool which shortens time-to-market for a complex SoC designs by the factor of 3x practically for any applications. It performs full automatic synthesis of digital systems from behavior specification to description in HDL at a Register Transfer Level (RTL). For description of system behaviour, Synthagate uses Algorithmic State Machines (ASMs) in two forms – graphical or System C. ASM hierarchical models and their transformations are used at all stages of behaviour and structure synthesis. The technology and concept is proven and implemented as a fast and powerful prototype and it allows rapid implementation, optimization, verification and estimation of multiple design versions. At the same time, it automatically generates the design documentation and specifications. Synthesized digital systems have high performance, small area, and power consumption.

Synthagate unique technology and prototype provides the highest QoR, practically unlimited Capacity, record Speed of synthesis, and removes most restrictions to users' design skill sets. Thus, Synthagate expands usability of its tools to all known structures of digital systems and to a much wider user base. All of this assures commercial success of this new 4th generation of the HLS tools. No such HLS tools are available from Synopsys, Cadence, or Mentor Graphics corporations. Several companies offer 3rd generation HLS tools that are primary focused on data path oriented digital systems and have multiple drawbacks.

Synthagate fast logic synthesis of complex Finite State Machines (FSM) and combinational circuits reduces the circuit area by as much as 50% as compared with results obtained by the best industrial tools from Synopsys, Cadence, Xilinx, Altera and Mentor Graphics. At the same time, Synthagate runs faster than other tools by a factor of 10 or more.