Chapter 8

LCD Controller

The Liquid Crystal Display (LCD) controller, which is incorporated into several devices in the MSP430 family (’3xx and ’4xx), provides a rapid and simple way to interface between a program and an LCD display. The LCD controller controls the LCD display, generating voltage signals for the segments. It supports static and multiplexed display interfaces (2 mux, 3 mux and 4 mux). This chapter describes in detail the LCD driver interface and LCD_A controller, both of which are implemented in the MSP430FG4618 device on the Experimenter's board.

Topic **Page**

8.1 LCD Controller Introduction

The LCD controllers supported by the '3xx and '4xx families drive LCD displays with a range of multiplex rates. Two LCD controllers are supported by the MSP430 microcontroller family. The first, known as the LCD controller, is supported by all MSP430x4xx devices. The second, known as LCD_A, is supported by the MSP430x42x0 and MSP430FG461x devices.

This chapter will focus on the operation of the LCD_A controller, because it is the one used by the MSP430FG4618 MCU fitted on the Experimenter's board.

Both LCD controllers include the following features:

- Display memory;
- Automatic signal generation;
- Configurable frame frequency;
- Blinking capability;
- Support for 4 types of LCDs:
  - Static;
  - 2-mux, 1/2 bias (or 1/3 bias for LCD_A controller);
  - 3-mux, 1/3 bias (or 1/2 bias for LCD_A controller);
  - 4-mux, 1/3 bias (or 1/2 bias for LCD_A controller).

8.1.1 Main differences between LCD and LCD_A controllers

The main differences between the two LCD controllers relate to their features. The LCD_A provides a regulated charge pump and allows contrast control by software. Additionally, for this driver, fractional LCD biasing voltages can be sourced internally or externally. The LCD controller requires external circuitry (a resistor-divider network) to generate up to 4 externally driven voltage levels (R03, R13, R23 and R33), which source the internal voltage generator.

With respect to the timing generator, the differences arise from the clock signal used for the LCD frequency. Whilst the LCD controller uses the timing generator sourced from Basic Timer 1 (see Chapter 8), the LCD_A controller uses ACLK to generate the timing for common and segment lines.

8.2 LCD_A Controller Operation

The LCD_A controller can be configured as the controller for the LCD, making use of external circuitry (a resistor-divider network). This generates up to 4 externally supplied voltage levels (R03, R13, R23 and R33), which source the voltage generators, V5, V4 and V3, V2 and V1 respectively. Additionally, the LCD Bias Generator can internally generate the fractional LCD biasing voltages, V2 – V5, independent of the source of V_{LCD}:

- R33 → V1: full-scale voltage (V_{LCD});
- R23 → V2: 2/3 of full scale;
- V3: 1/2 of full scale (LCD_A controller only);
- R13 → V4: 1/3 of full scale;
- R03 → V5: ground.

The following table gives the LCD Voltage and Biasing Characteristics of the LCD_A controller:

Table 8-1. LCD_A controller naming convention, LCD Voltage and Biasing Characteristics.

Mode	Bias conf.	LCD_A controller							
		LCDMXx	LCD2B	COM	V1	V2	V3	V4	V5
Static	Static	00	X	1	X				X
2-mux	1/2	01	1	2	X		X		X
2-mux	1/3	01	0	2	X	X		X	X
3-mux	1/2	10	1	3	X		X		X
3-mux	1/3	10	0	3	X	X		X	X
4-mux	1/2	11	1	4	X		X		X
4-mux	1/3	11	0	4	X	X		X	X

Although LCD and LCD_A controllers use different clock signals to source the timing generator, the LCD_A circuit sources the analogue voltage multiplexer that generates the control signals for the multiplexers.

Because the LCD_A controller uses the user selectable ACLK (32768 Hz) prescaler, selected with the LCDFREQx bits, the appropriate LCD frequency, f_{LCD}, depends on the framing frequency, f_{frame}, and multiplex rate, mux, defined on the LCD specifications. The LCD frequency should be configured according to the following equation:

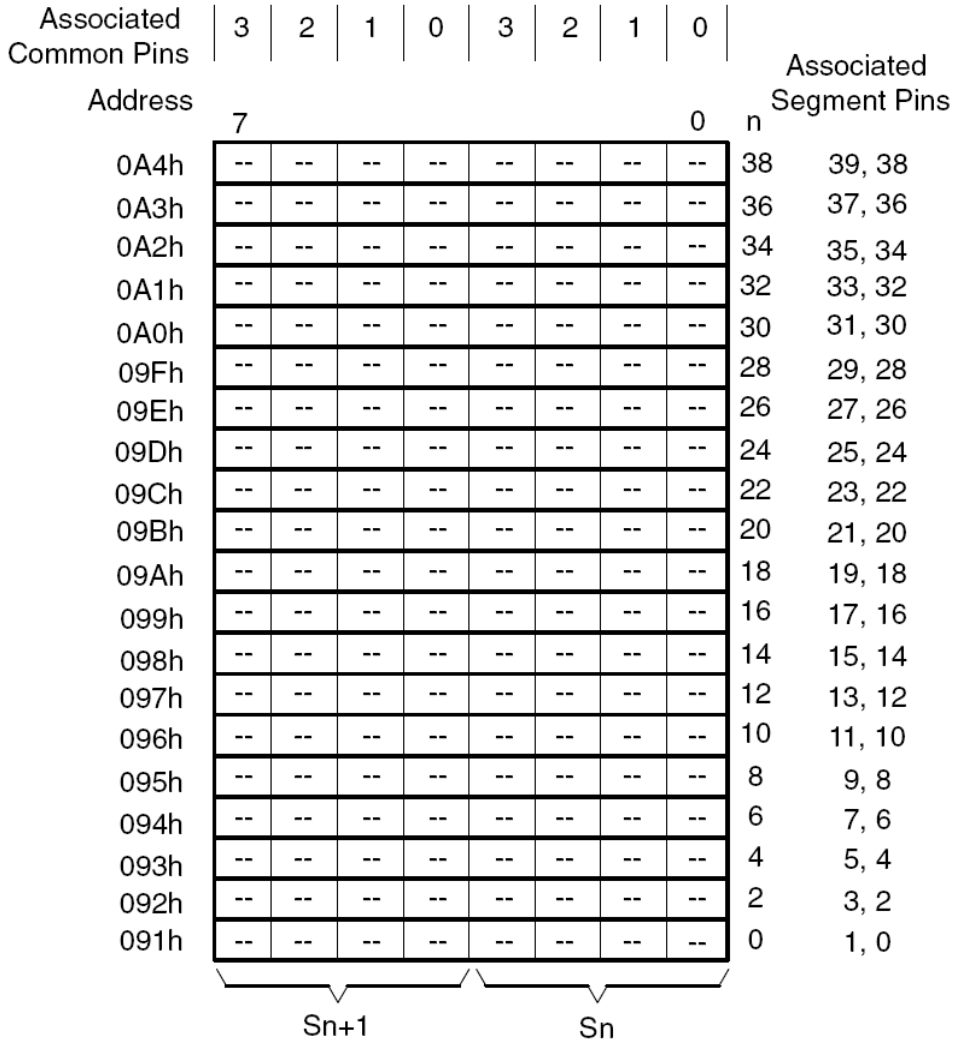
$$f_{LCD} = 2 \times mux \times f_{frame}$$

8.2.1 LCD Memory

The LCD memory map is shown in *Figure 8–1*. Depending on the LCD type (Static, 2-mux, 3-mux or 4-mux) and on the device, each LCD segment is turned on by setting its corresponding memory bit.

The maximum number of segment lines available depends on the device. Refer to the appropriate device-specific data sheet for the available segment pins.

Figure 8-1. LCD Memory Map.



8.2.2 Blinking the LCD

The LCD controller supports blinking. The LCDSON bit is ANDed with the memory bit of each segment. When LCDSON = 1, each segment is on or off, depending on the value of its memory bit. When LCDSON = 0, each LCD segment is turned off.

8.2.3 LCD_A Voltage and Bias Generation

In addition to internal voltage generation, both the peak output waveform voltage, V1, as well as the fractional LCD biasing voltages V2 – V5 can be sourced externally.

- To use the internal voltage generator:
  - OSCOFF = 1: Oscillator sourcing ACLK set;
  - LCDON = 1: LCD_A module active;
    - V_{LCD} may be sourced internally from AV_{CC} or from an internal charge pump.
- To source V_{LCD} externally, the above bits must be disabled.

LCD Voltage Selection

V_{LCD} source:

- AV_{CC} requires:
  - VLCDEXT = 0;
  - VLCDx = 0;
  - VREFx = 0.
- Internal charge pump sourced from DV_{CC} requires:
  - VLCDEXT = 0;
  - VLCDPEN = 1;
  - VLCDx > 0 (software selectable LCD voltage from typically 2.60 V to 3.44 V: independent of DV_{CC});
  - Connect a 4.7 μF or larger capacitor between pin LCDCAP and ground.

LCD Bias Generation

- Generation of external fractional LCD biasing voltages, V2 – V5:
  - REXT = 1;
  - External equally weighted resistor divider network, with resistor values between 100 kΩ and 1 MΩ;
  - VLCDEXT = 0: The V_{LCD} voltage is sourced from the internal charge pump, with R33 providing a switched-V_{LCD} output. Otherwise (VLCDEXT = 1), R33 provides a V_{LCD} input.
  - R03EXT = 1: V5 is sourced externally.
- Internal bias generator:
  - When LCD2B = 1, it supports 1/2 bias LCDs.
  - When LCD2B = 0, it supports 1/3 bias LCDs in 2-mux, 3-mux, and 4-mux modes. In static mode, the internal divider network is disabled;
  - For LCD devices that share the LCDCAP, R33, and R23 functions, the charge pump cannot be used with an external resistor divider with 1/3 biasing;
  - When R03 is not available externally, V5 is always AV_{SS}.

8.2.4 LCD Contrast Control

The VLCDx selection controls the LCD contrast by adjusting the LCD voltage generated by the integrated charge pump.

- The contrast of the LCD depends on the:
  - Peak voltage of the output waveforms;
  - Selected mode;
  - Biasing.
- The contrast ratio of the LCD depends on the:

- LCD display;
- Selected biasing scheme.

8.2.5 LCD Timing Generation

- LCD frequency, f_{LCD}, depends on the:
  - Framing frequency;
  - LCD multiplex rate;
  - Selectable with the LCDFREQx bits.

$f_{LCD} = 2 \times mux \times f_{frame}$

8.3 LCD modes

The LCD_A controller supports 4 types of LCD devices:

- Static:
  - Each MSP430 segment pin drives one LCD segment;
  - One common line driven by COM0;
  - Capacity to drive 32 segments.
- 2-mux, 1/2 bias (or 1/3 bias for LCD_A controller):
  - Each MSP430 segment pin drives two LCD segments;
  - Two common lines driven by COM0 and COM1;
  - Capacity to drive 64 segments.
- 3-mux, 1/3 bias (or 1/2 bias for LCD_A controller):
  - Each MSP430 segment pin drives three LCD segments;
  - Three common lines driven by COM0, COM1, and COM2;
  - Capacity to drive 90 segments.
- 4-mux, 1/3 bias (or 1/2 bias for LCD_A controller):
  - Each MSP430 segment pin drives four LCD segments
  - Four common lines driven by COM0, COM1, COM2, and COM3;
  - Capacity to drive 160 segments.

8.3.1 Static Mode

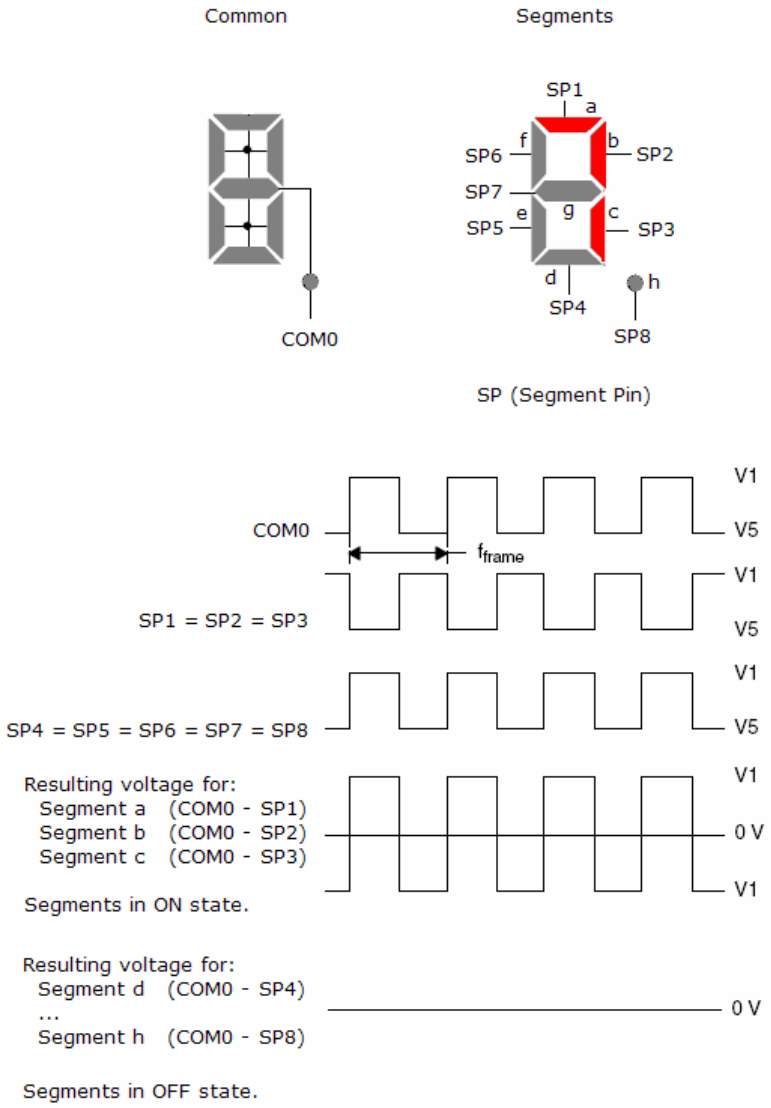
A static LCD has one pin for each segment and one pin for the backplane. This type of LCD has a high contrast ratio but requires a large number of pins.

Example: Display the number "7" on the LCD

To display the number "7" on the LCD, segments a, b and c must be turned on. The waveforms at pins SP1, SP2 and SP3 (see *Figure 8-*

2), must be the inverse of the waveform at the common pin (COM0), so these segments are in the ON state. The waveforms at the remaining segment pins must be the same as the common pin waveform, to obtain the OFF state. *Figure 8–2* shows an example of a static waveforms to display the number "7".

Figure 8-2. Static LCD waveforms – example: display number "7".



Additional details are given in the MSP430x4xx Family User's Guide <*slau056g.pdf*>.

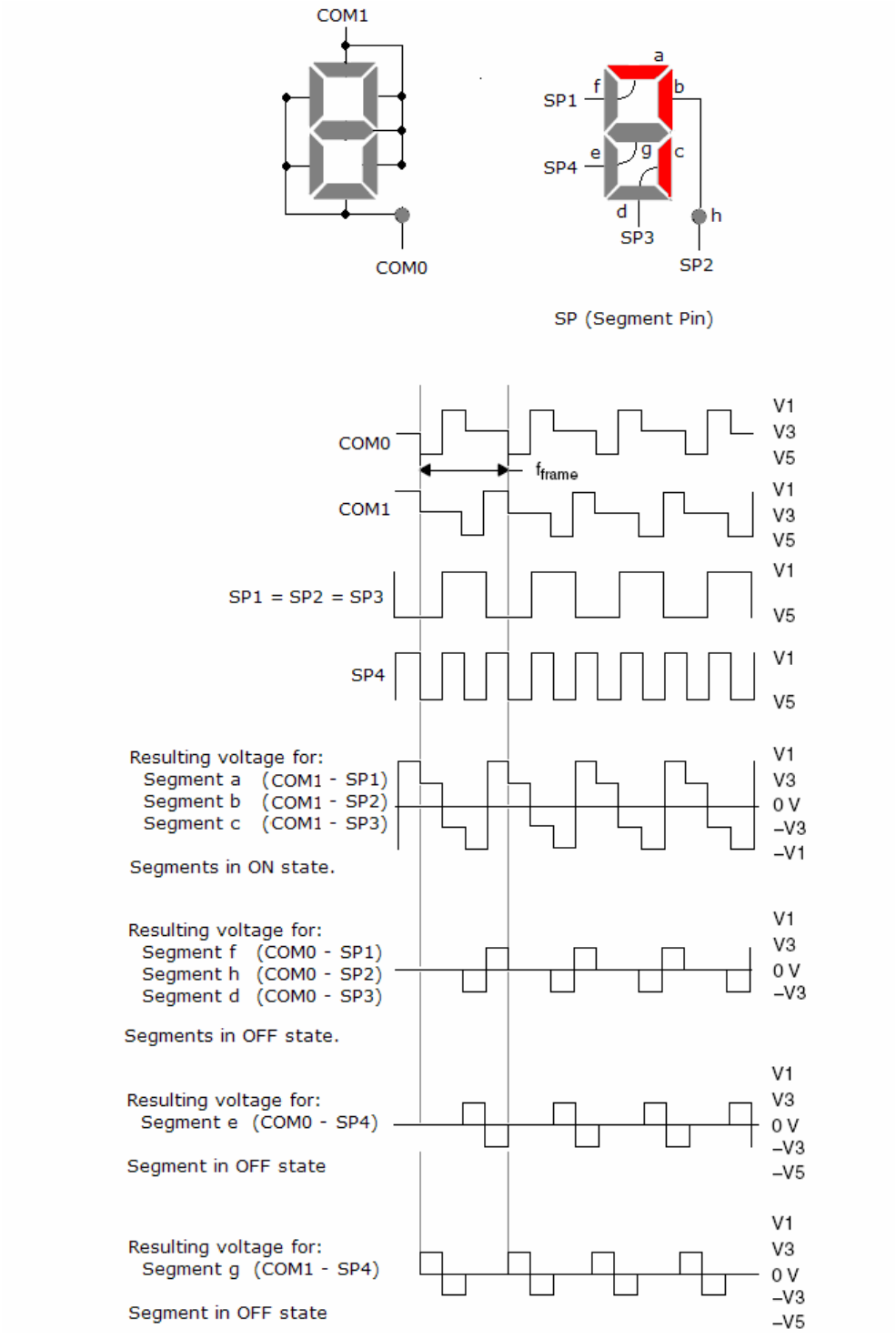
8.3.2 2-Mux Mode

To reduce the pin count, there are LCDs where the segments are multiplexed. In the case of a 2-mux LCD, the individual LCD segments are arranged in a matrix, with two common pins (COM0 and COM1). This type of LCD requires half the pin count of a static LCD.

Example: Display the number "7" on the LCD

To display the number "7" on the LCD, segments a, b and c must be turned on. The waveforms at pins, SP1, SP2 and SP3 (see Figure 7-3) must be time-division-multiplexed. The voltage signals that use combined common pins (COM0 or COM1) turn these segments ON by applying the voltage V1. The resulting voltage waveforms at the remaining segment pins must be lower than the LCD segment driving voltage (V1), in order to achieve the OFF state. *Figure 8–3* shows an example of 2-mux, 1/2 bias, waveforms for displaying the number "7".

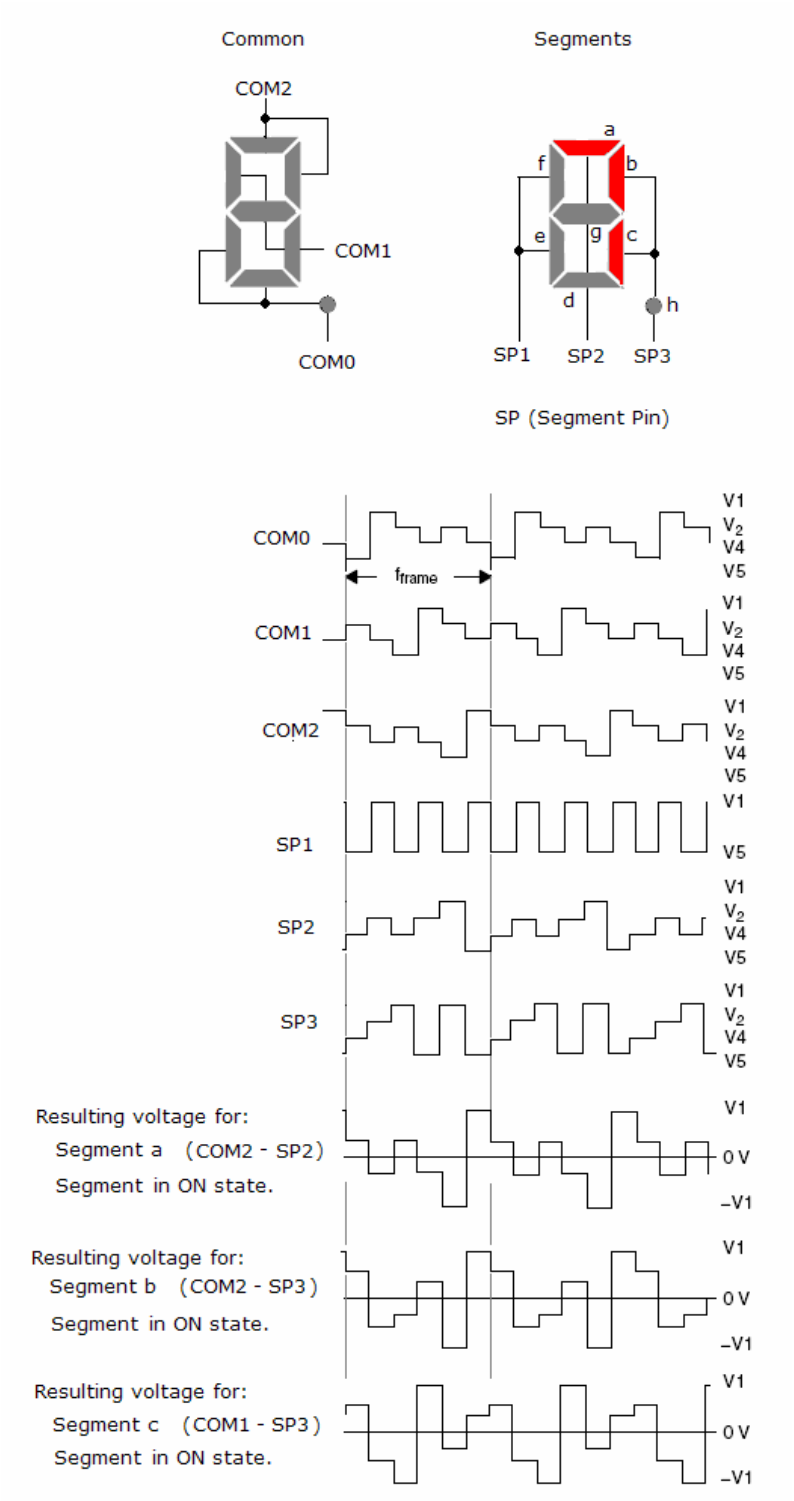
Figure 8-3. 2-mux LCD waveforms – example: display number "7".



8.3.3 3-Mux Mode

In 3-mux mode, the MSP430 segment pins drive three LCD segments and three common lines (COM0, COM1, and COM2). This increases the number of available segments, without increasing the pin count. In *Figure 8-4* shows a 3-mux LCD waveform – example: the number "7".

Figure 8-4. 3-mux LCD, 1/3 bias, waveforms – example: display number "7".



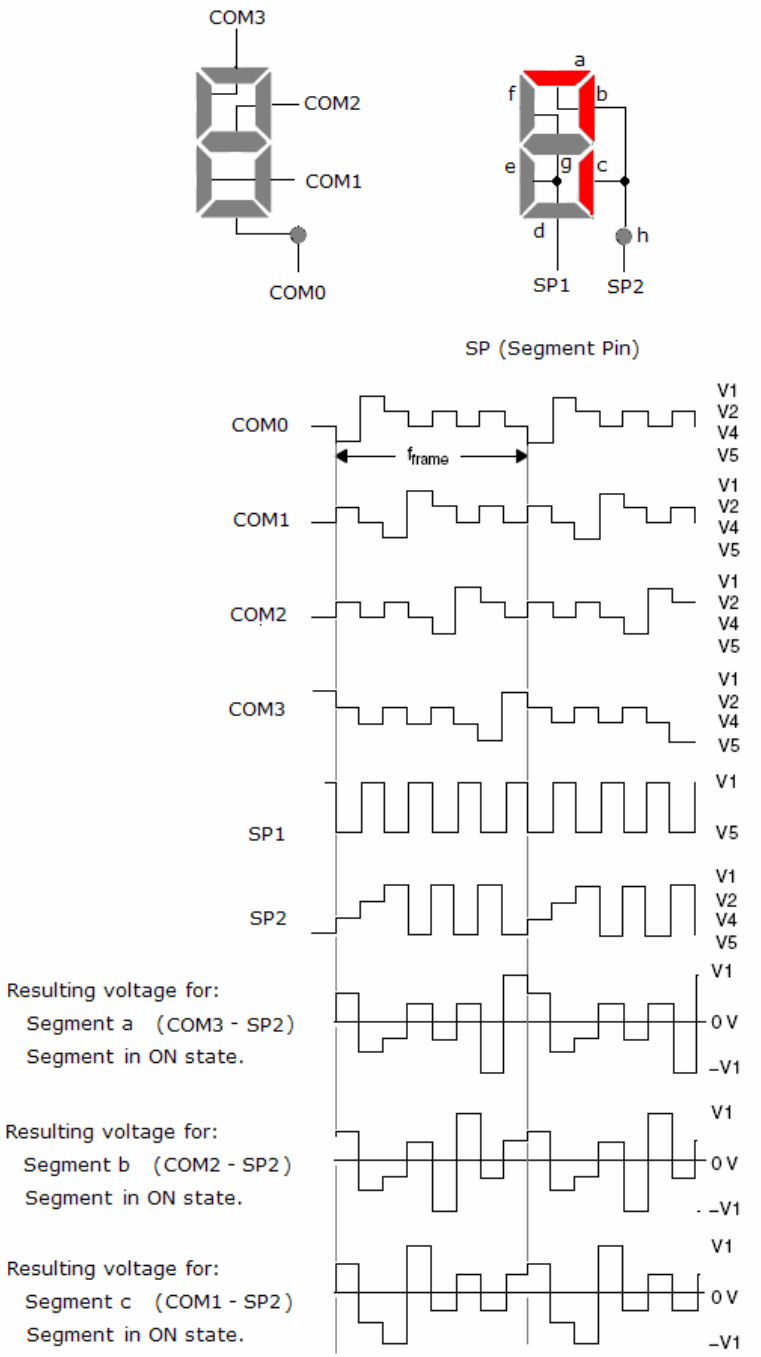
The remaining segments are in the OFF state, producing different waveforms varying between –V4 and V4, with voltages that cannot drive the LCD.

8.3.4 4-Mux Mode

In 4-mux mode, the MSP430 segment pins drive four LCD segments and four common lines (COM0, COM1, COM2, and COM3).

Figure 8–5 shows an example 4-mux, 1/3 bias LCD waveforms – example: number "7".

Figure 8-5. 4-mux LCD, 1/3 bias, waveforms – example: display number "7".



As in the previous example, the additional segments are in the OFF state, generating different waveforms varying between –V4 and V4 voltages that cannot drive the LCD.

8.4 Registers

LCDACTL, LCD_A Control Register

7	6	5	4	3	2	1	0
LCDFREQx			LCDMXx		LCDSON	Unused	LCDON

Bit		Description
7 - 5	LCDFREQx	LCD Frequency Select by ACLK divider configuration: LCDFREQ2 LCDFREQ1 LCDFREQ0 = 000 ⇒ ACLK / 32 LCDFREQ2 LCDFREQ1 LCDFREQ0 = 001 ⇒ ACLK / 64 LCDFREQ2 LCDFREQ1 LCDFREQ0 = 010 ⇒ ACLK / 96 LCDFREQ2 LCDFREQ1 LCDFREQ0 = 011 ⇒ ACLK / 128 LCDFREQ2 LCDFREQ1 LCDFREQ0 = 100 ⇒ ACLK / 192 LCDFREQ2 LCDFREQ1 LCDFREQ0 = 101 ⇒ ACLK / 256 LCDFREQ2 LCDFREQ1 LCDFREQ0 = 110 ⇒ ACLK / 384 LCDFREQ2 LCDFREQ1 LCDFREQ0 = 111 ⇒ ACLK / 512
4 - 3	LCDMXx	LCD mux rate for LCD mode setting: LCDMX1 LCDMX0 = 00 ⇒ Static LCDMX1 LCDMX0 = 01 ⇒ 2–mux LCDMX1 LCDMX0 = 10 ⇒ 3–mux LCDMX1 LCDMX0 = 11 ⇒ 4–mux
2	LCDSON	LCD segments on when LCDSON = 1.
0	LCDON	LCD_A module active when LCDON = 1.

LCDAPCTL1, LCD_A Port Control Register 1

7	6	5	4	3	2	1	0
Unused						LCDS36	LCDS32

Bit		Description
1	LCDS36	LCD Segment 36 to 39 Enable.
0	LCDS32	LCD Segment 32 to 35 Enable.

LCDAPCTL0, LCD_A Port Control Register 0

7	6	5	4	3	2	1	0
LCDS28	LCDS24	LCDS20	LCDS16	LCDS12	LCDS8	LCDS4	LCDS0

Bit		Description
7	LCDS28	LCD Segment 28 to 31 Enable.
6	LCDS24	LCD Segment 24 to 27 Enable.
5	LCDS20	LCD Segment 20 to 23 Enable.
4	LCDS16	LCD Segment 16 to 19 Enable.
3	LCDS12	LCD Segment 12 to 15 Enable.
2	LCDS8	LCD Segment 8 to 11 Enable.
1	LCDS4	LCD Segment 4 to 7 Enable.
0	LCDS0	LCD Segment 0 to 3 Enable.

LCDAVCTL0, LCD_A Voltage Control Register 0

7	6	5	4	3	2	1	0
Unused	R03EXT	REXT	VLCDEXT	LCDCPEN	VLCDREFx		LCD2B

Bit		Description
6	R03EXT	V5 voltage select: R03EXT = 0 ⇒ V5 is AV_{SS}. R03EXT = 1 ⇒ V5 is sourced from the R03 pin.
5	REXT	V2 – V4 voltage source selection: REXT = 0 ⇒ V2 – V4 are generated internally. REXT = 1 ⇒ V2 – V4 are sourced externally
4	VLCDEXT	V_{LCD} source select: VLCDEXT = 0 ⇒ V_{LCD} is generated internally. VLCDEXT = 1 ⇒ V_{LCD} is generated externally.
3	LCDCPEN	Charge pump enable: LCDCPEN = 0 ⇒ Charge pump disabled. LCDCPEN = 1 ⇒ Charge pump enabled when VLCDEXT = 0 and VLCDx > 0 or VLCDREFx > 0.
2 – 1	VLCDREFx	Charge pump reference select: VLCDREF1 VLCDREF0 = 00 ⇒ Internal. VLCDREF1 VLCDREF0 = 01 ⇒ External. VLCDREF1 VLCDREF0 = 10 ⇒ Reserved. VLCDREF1 VLCDREF0 = 11 ⇒ Reserved.
0	LCD2B	Bias select (for any of the mux modes): LCD2B = 0 ⇒ 1/3 bias. LCD2B = 1 ⇒ 1/2 bias.

LCDAVCTL1, LCD_A Voltage Control Register 1

7	5	4	3	2	1	0
Unused		VLCDx				Unused

Bit		Description		
4 - 1	VLCDx	Charge pump voltage select:		
		VLCD3 VLCD2 VLCD1 VLCD0 = 0000	⇒	Disable.
		VLCD3 VLCD2 VLCD1 VLCD0 = 0001	⇒	V_{LCD} = 2.60 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 0010	⇒	V_{LCD} = 2.66 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 0011	⇒	V_{LCD} = 2.72 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 0100	⇒	V_{LCD} = 2.78 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 0101	⇒	V_{LCD} = 2.84 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 0110	⇒	V_{LCD} = 2.90 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 0111	⇒	V_{LCD} = 2.96 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1000	⇒	V_{LCD} = 3.02 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1001	⇒	V_{LCD} = 3.08 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1010	⇒	V_{LCD} = 3.14 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1011	⇒	V_{LCD} = 3.20 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1100	⇒	V_{LCD} = 3.26 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1101	⇒	V_{LCD} = 3.32 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1110	⇒	V_{LCD} = 3.38 V.
		VLCD3 VLCD2 VLCD1 VLCD0 = 1111	⇒	V_{LCD} = 3.44 V.

8.5 Laboratory 4: LCD message display

This hands-on laboratory consists of configuring the LCD_A controller of the MSP430FG4618 device of the Experimenter's board to display a message on the LCD display. As in the case of the previous exercise (Lab3), this laboratory is composed of some sub-tasks. This laboratory has been developed for *Code Composer Essentials version 3* software development tool only.

Project files

- C source files: **Chapter 8 > Lab4 > Lab4_student.c**
  Chapter 8 > Lab4 > LCD_defs.h
- Solution file: **Chapter 8 > Lab4 > Lab4_solution.c**

Overview

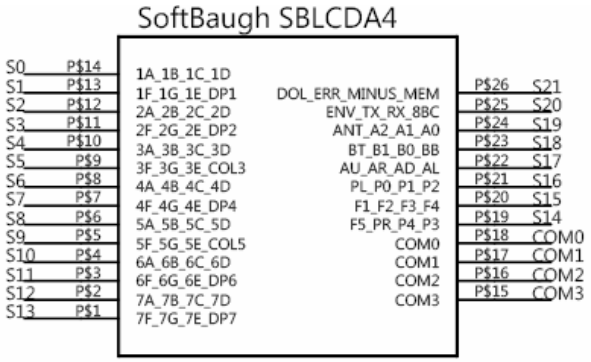
This laboratory will explore the LCD_A controller of the MSP430FG4618 device included on the Experimenter's board. This application demonstrates the activation of various LCD segments.

A. Resources

The Experimenter's board uses a LCD, which does not have its own controller. The operation is controlled by MSP430FG4618. The interface between these two components is described in the Experimenter's Board datasheet. It is also recommended that the LCD datasheet be read.

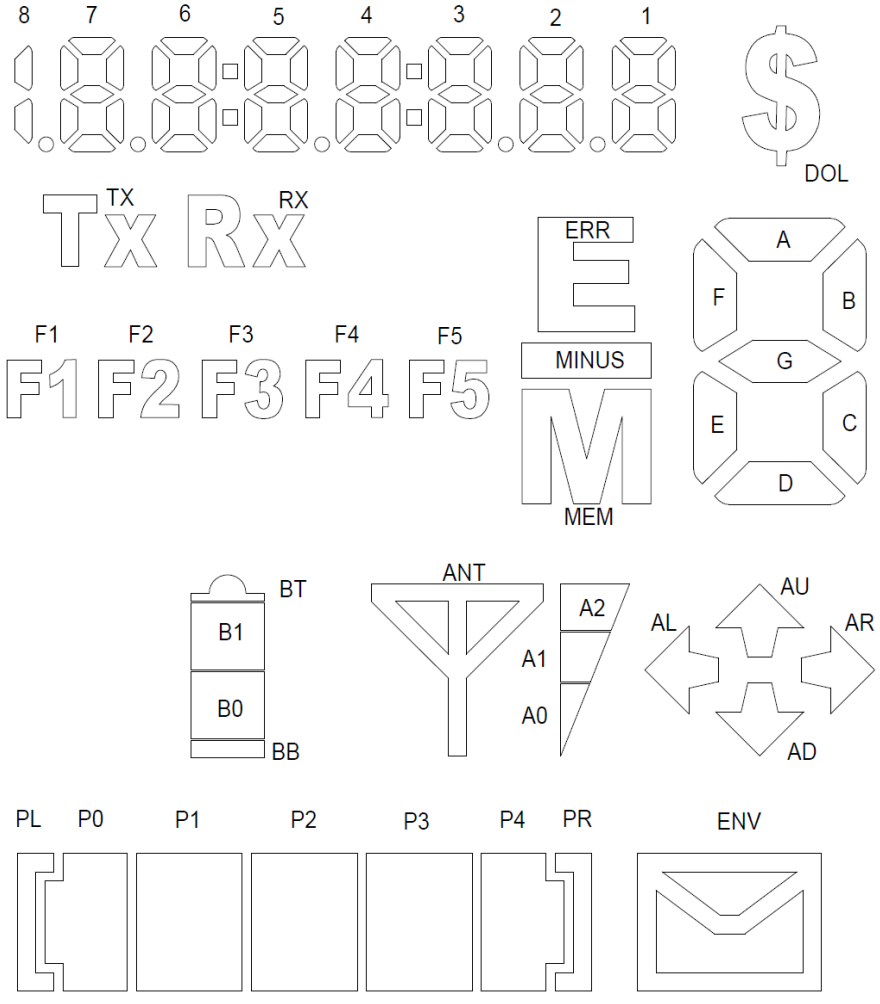
The *Figure 8-6* shows the connections between the two devices.

Figure 8-6. Connections between the MSP430FG4618 and the Softbaugh LCD SBLCDA4.



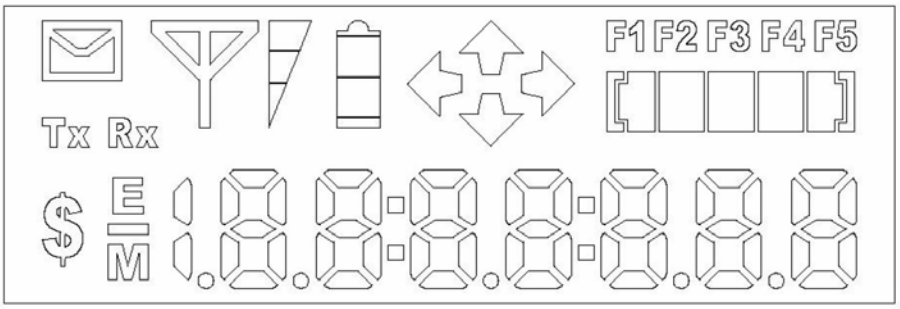
The description of each segment is shown in *Figure 8-7*.

Figure 8-7. Softbaugh LCD SBLCDA4 segments description.



The information is organized in the LCD as shown in *Figure 8-8*.

Figure 8-8. Softbaugh LCD SBLCDA4 segments display.



Based on this information, it is possible to define the values to write to each of the memory registers to turn on the desired segments, or to set several of them, as is the case with numbers. The definitions are listed in the Annex to this laboratory.

From analysis of the Experimenter's Board schematics, it can be seen that there is a 10 μF between the LCDCAP pin and ground, which means it is possible to use the charge pump.

The segments shared by the I/O function are not used by the LCD, being connected to the segments S4 to S25. The four lines COM0, COM1, COM2, and COM3 are used. The last three lines are shared by ports P5.2, P5.3 and P5.4, respectively. The LCD is operated in 4-mux mode.

The pins R03, R13, R23 and LCDCAP\R33 are used to provide the V5, V4, V3, V2 and V1 (VLCD) voltages, using an external resistor network. They are available at Header H5.

In the current Experimenter's Board configuration, it is possible to select the AVss or charge pump to provide the V1 (VLCD), V2, V3, V4 and V5 voltages. These voltages are only generated when LCD_A module and the ACLK clock are active. This allows the use of low power mode 3 (LPM3).

Timer_A, together with the TACCR0 unit are used to generate an interrupt once every second. LED1 and LED2 are switched at each Timer_A interrupt.

The push button SW1 is used to change the value of voltage generated by the charge pump. The push button SW2 is used to change the LCD frequency.

B. Organization of software application

The application starts by configuring the Ports P5.2, P5.3, P5.4 to special function COM1, COM2 and COM3, respectively. The function of COM0 is not shared with the digital I/O functions.

Then, the pins with multiplexed functions are selected to perform the functions necessary to control the LCD segments.

The LCD_A control register and the voltage configuration register are also configured.

There then follows the execution of the LCD clear routine ***LCD_all_off()***, which ensures that all segments of the LCD are off.

Timer_A is configured with its TACCRO unit to generate an interrupt once every second. The ISR generates the memory clock with msec, sec and min, and also connects/disconnects the remaining LCD symbols.

The port pins P2.1 and P2.2 drive LED2 and LED1, respectively. Hence, these ports are configured as digital outputs.

Push buttons SW1 and SW2 have the capacity to generate an interrupt through a change at ports P1.0 and P1.2 respectively. The interrupt ISR, after decoding its source, modifies the LCD operation frequency or modifies the VLCD voltage.

Finally, all the interrupts are activated and the system enters low power mode LPM3.

C. System configuration

- **LCD_A interface with the LCD configuration**

Select the function COM1, COM2 and COM3. What is the value to write to these registers?

```
P5DIR | = _________________;
P5SEL | =_________________;
```

The LCD segments are controlled by the S4 to S25 LCD memory segments. Activate these segments by writing to correct value to the following register:

```
LCDAPCTL0 = _______________;
```

❑ LCD operation frequency

The LCD is to operate in 4-mux mode, with a 30 Hz to 100 Hz refresh frequency. It uses the following equation to determine the LCD operation frequency, f_{LCD}:

$f_{LCD} = 2 \times mux \times f_{frame}$

Choose the frequency that provides greatest energy savings.

❑ LCD_A configuration

The LCD_A module is to be activated in 4-mux mode from a 32768 Hz clock. What value should be written to the following register?

```
LCDACTL = _____________________;
```

Use the charge pump to internally generate all the voltages necessary for the operation of the LCD, using a bias 1/3. What is the value to write to the register?

```
LCDAVCTL0 = _____________________;
```

The charge pump generates a LCD voltage of 3.44 volts. Configure the following register:

```
LCDAVCTL1 = _____________________;
```

❑ Timer_A configuration

The Timer_A generates an interrupt once every second. It uses the TACCR0 unit. Configure the following registers:

```
TACCTL0 = _____________________;
TACCR0 = _____________________;
TACTL = _____________________;
```

❑ Output ports configuration

Configure the ports connected to LED1 and LED2 in order to make one of them active and the other inactive at system start up:

```
P2DIR |= _____________________;
P2OUT |= _____________________;
```


❑ **Input ports configuration**

The push buttons SW1 and SW2 generate an interrupt on a low-to-high transition. Configure the necessary registers:

```
P1DIR |= ____________________________;
P1IES = ____________________________;
P1IE |= ____________________________;
```

D. Operation analysis

Compile the project, load it into microcontroller's memory and execute the application. For each value of the operating frequency and voltage generated by the charge pump, measure the electrical current consumption. Draw a graph of these results and draw conclusions concerning the energy consumption.

MSP-EXP430FG4618 **SOLUTION**

Configure the LCD_A controller of the MSP430FG4618 device of the Experimenter's board to display a message on the display.

❑ LCD_A interface with the LCD configuration:

```
P5DIR |= 0x1E;   // Ports P5.2, P5.3 and
                 //P5.4 as outputs
P5SEL |= 0x1E;   // Ports P5.2, P5.3 and P5.4 as
                 // special function (COM1, COM2 and COM3)
LCDAPCTL0 = LCDAPCTL0 = LCDS24 | LCDS20 | LCDS16 | LCDS12
| LCDS8 | LCDS4;                  // Enable S4 to S25
```

❑ LCD operation frequency:

```
LCDACTL = LCDFREQ_192 | LCD4MUX;    // (ACLK = 32768)/192
                                    // and 4-mux LCD
```

❑ LCD_A configuration:

```
LCDACTL |= LCDSON | LCDON;     // LCD_A on and Segments on
LCDAVCTL0 = LCDCPEN;           // Charge pump enable
LCDAVCTL1 = VLCD_3_44;         // VLCD = 3.44 V
```

❑ Timer_A configuration:

```
TACCTL0 = CCIE;         // TACCR0 interrupt enabled
TACCR0 = 3268;          // this count correspond to 1 msec
TACTL = TASSEL_1 + MC_1 + ID_0;  // ACLK, up mode
```

- Output ports configuration:

```
P2DIR |= 0x06;                  // P2.1 and P2.2 as output
P2OUT |= 0x04;                  // LED2 off and LED1 on
```

- Input ports configuration:

```
P1DIR &= ~0x03;       // P1.0 and P1.1 digital inputs
P1IES |= 0x03;        // low-to-high transition interrupts
P1IE |= 0x03;         // enable port interrupts
```

8.6 Quiz

1. The fractional LCD biasing voltages V2, corresponds to which fraction of full-scale voltage?

(a) 1/1;

(b) 1/2;

(c) 2/3;

(d) 1/3.

2. To blink the LCD, the following LCD_A control register bit must be set:

(a) LCDON;

(b) LCDSON;

(c) LCDCPEN;

(d) LCD2B.

3. To source the fractional LCD biasing voltages externally:

(a) Reset OSCOFF and LCDON bits;

(b) Set OSCOFF bit;

(c) Reset LCDON bit;

(d) Set OSCOFF and LCDON bit.

4. To configure a LCD period of approximately 10 milliseconds:

(a) LCDMXx = 1;

(b) LCD2B = 1;

(c) LCDFREQx = 3;

(d) LCDFREQx = 7.

5. An LCD with 3-mux, 1/3 bias configuration requires:

(a) LCDMXx = 2 and COM = 3;

(b) LCD2B = 0;

(c) All of the above;

(d) None of the above.

6. An LCD with 3-mux, 1/2 bias has the capacity to drive:

(a) 90 segments;

(b) 160 segments;

(c) 140 segments;

(d) 64 segments.

Solution: 1. (c); 2. (b); 3. (a); 4. (d); 5. (c); 6. (a)

8.7 FAQs

1. What is the maximum number of segment lines controllable using the LCD_A controller?

The maximum number of segment lines available differs between devices. See the device-specific datasheet for details.

2. LCDSx Bits affect dedicated LCD segment pins?

No. The LCDSx bits only affect pins with multiplexed LCD segment functions and digital I/O functions.

3. What should be the capacitor value for the internal charge pump?

It is recommended that a 4.7 µF capacitor or larger is connected between the LCDCAP pin and ground.