Beginners manual for Cadence

Starting the Cadence for the first time.

```
vahvel:/home/elmet>cd testcad
/home/elmet/testcad
vahvel:/home/elmet/testcad>ams_cds -mode fb -tech csx
ams_cds: Command not found.
vahvel:/home/elmet/testcad>cad
Select your CAD tools:
1) CADENCE
2) MENTOR
3) SYNOPSYS
4) CADENCE & SYNOPSYS
5) MENTOR & SYNOPSYS
5) MENTOR & SYNOPSYS
0) no selection
----> 1
Environment ready for Cadence.
vahvel:/home/elmet/testcad>ams_cds -mode fb -tech csx
icfb : HIT-Kit=3.40 tech=csx tool=artist
```

Drawing 1: Cadence initialization (terminal window)

Follow these steps [Drawing 1]:

- create new subdirectory (use 'mkdir' command for this purpose)
- change working directory to this subdir (command 'cd <dirname>')
- run environment setup script (command 'cad') and choose the package you'll going to use
- run Cadence as follows: 'ams cds -mode fb -tech csx'

As you can see from the picture, trying to run cadence without 'cad' command doesnt work.

For using newest version (if you feel like experimenting) then do this (until the newest installation becomes system default):

- first two steps are the same
- do 'setenv CADENCE_05' OR 'export CADENCE_05' (this depends on the shell you're using, if one doesnt work – try another)
- let system script set your environemnt variables for the use of Cadence (command 'source /cad/cadrc.include')
- run Cadence as follows: 'ams_cds -mode fb -tech cxq' (note the difference in technology selection option – HRDLIB may and will be different for each tech) and select 'CXQ' from the technology selection dialog.

If all is well - several windows will pop up, windows named 'icfb' and 'Library Manager' among those. Cadence Graphical User Interface (GUI) has been under very conservative development so there is'nt much difference between versions.

Starting to work on new circuit

You'll probably have to create new library (for storing circuit modules) and at least one cellview (selected circuit module). Follow these steps:

- create new library using 'Library Manager' window [Drawing 2]



Drawing 2: Library manager - new library

define new library name and choose techfile [Drawing 3, Drawing 4, Drawing 5] _

Library	OK Cancel	Holn
Name test		пер
Directory	Technology File for library "test"	
•••	If you will be creating mask layout other physical data in this library, will need a technology file. If your	t or you alan
/home/elmet/testcad	to use only schematic or HDL data	i, a
Design Manager	technology file is not required.	
Use NONE Use No DM	You can: Compile a new techfile Attach to an existing t	e techfile
OK Apply Cancel Help	Don't need a techfile Drawing 4: Technology selection, st	tep 1

Drawing 3: Create new library

ок	Cancel	Defaults	Apply	Help
New Desi	(pi Library	2	test	
Technoloį	jy Library		LEADFRAMES TECH_CSI US_8ths analogLib basic cdsDefTechLib functional sbaLib	

Drawing 5: Technology selection, step 2

Choose appropriate technology, TECH_CSI or cdsDefTechLib.

- create new cell view (open menu on the Library Manager window and enter cell name, as seen on [Drawing 6, Drawing 7]



Drawing 6: Creating new cellview, step 1

ок	Cance	el	Defaults		Help					
Library N	ame		test							
Cell Name		te	estcell							
View Nan	ne	schematic								
Tool		Composer-Schematic —								
Library path file										
/home/elmet/testcad/cds.lib										

Drawing 7: Creating new cellview, step 2

After this, circuit editor window appears [Drawing 8]. You can now start working on your design. Preferred work order should be following:



Drawing 8: Editor window

- place instances [Drawing 9], instances should all stem from library 'HRDLIB'. Keyboard shortcut for this is 'i'.

1	Cma	d: Instanc	e	Sel:	0												_	4
h	Tools	Design	Window	Edit	Add	Check	Sheet	Options	HIT-KIT	Utilities							Hel	Ip
ŀ														 			·	
	H																	
	~																	
	€																	
ŀ	\sim																	
	्र							<u>4</u>	IØ									
k								AND)									
	120								I1									
	\approx							ANDS) _ • ` `									
ŀ	~ k							ن ــــا										
	34							4	12									
ŀ)									
	t 1								13									
								AND)									
	國豪																	
							Add	Instan	Te		,							
l n	* etonor			ide	Can	rel De	faults				lein							
1	-			iuc -	Count		Tettino			!	icib							
l	EN I		Libr	ary	HRDL	ΙĘ				Brov	vse							
	-		Cell		AND 2	ř.				i —		· .						
	abc		Vie		symb	olį				ļ		· · ·						
ŀ					Y													
ľ	•->		Nar	nes	.1.													
ŀ			Arr	ay		Row	/s 1		Columns	1								
				Detet			0:-1-			Incide D								
11				notati			2106	ways		JUSIDE DI	nwn							_

Drawing 9: Instances

 place I/O pins. These pins could be single wires or buses. Bus notation is written as 'pin_name<start_index:end_index>'. See [Drawing 10].

Cm	d: Pin		Sel	: 0																										4
Tools	Design	Wind	ow	Edit	Add	Che	ck	Sheet	Opti	ons	HIT	-кіт	Utili	ties															He	elp
											į			÷.				Ľ.	Ċ.	į										
N																														
\checkmark																														
⊕²																														
~																														
Q ²									4			IØ																		
										AND2	-																			
\b>									-1_																					
									ė.			I1																		
\mathbb{R}										ANDZ	F.																			
												15																		
34									<u> </u>			12																		
									<u></u>	ANDS																				
f 1												13																		
										ANDZ	-																			
									- -[
1															·															
			_						A	dd I	Pin																			
		. fr	Lliz	lo (Conc	ol	Dofe	ulte										Це	de											
_		- -		IC .	Can	.61	Dere	unts										110	ab.											
- PN			Pin M	lames	2	A	<0:0	3> B <o< th=""><th>:3></th><th></th><th></th><th></th><th></th><th></th><th>_</th><th>_</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></o<>	:3>						_	_														
_	· ·	· .		icarrie.	•														_											
abc			Direc	tion:			inp	ut r		Bus	Expa	ansio	n 🔘) off) on														
		٠.	lear	10		sc	hem	natic 🗆		Place	amo	nt		i cin	oln		mul	ltink	.											
•->			, sai							That	Sinci			311	gic		ma	rapi	-											
DY.		. 1	B	otate					Sid	eway	/s					Ups	ide	Dov	/n											
Pin										-																				
\sim	mouse L	: mou	iseA	ddPti	0				M:	sch	HiM	ouseB	opU	p()					R	Ro	tat	te !	90							
C‡	Point at	locati	on p	oint f	or the	e pin.																								
							-				-		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Drawing 10: Adding pins

Direction field determines signal direction. Menu shorcut 'p'.

create connections [Drawing 11] Note there are thin and thick wires (single signals and buses).
 For separating single signal or group of signals from bus, the wires have to have names. This solves the problem what signal should go where.



Drawing 11: Wires and names



- finished circuit [Drawing 12]. Check and save it before doing any further operations.

Drawing 12: Finished circuit

Now there are several possibilities. You can use this circuit as building block for even more complex circuit (as macro), run simulation in Cadence or export it for external tools like Turbo Tester. First, marco creation.

Generating macro (symbol) from cellview.

This operation takes several steps:

- make cellview from cellview



Drawing 13: Create symbol, step 1

- Cellview generation confirmation, step 2 [Drawing 14]. You can select different design here.

OK Cance	el Defaults App	ly	Help
Library Name	test		Browse
Cell Name	testcell		
From View Name	schematic —	To View Name	symbol
		Tool / Data Type	Composer-Symbol 📼
Display Cellview			
Edit Options			

Drawing 14: Cellview from cellview

- Symbol options, step 3 [Drawing 15]. Set pin locations for macro box.

OK Cancel	Apply				Help
Library Name test		Cell Name testcell <u>i</u>		View Name symbol <u>i</u>	
Pin Specificatio	ns				Attributes
Left Pins	A<0:3> B<0:3>	Ľ			List
Right Pins	¥<0:3> <u>ĭ</u>				List
Top Pins	Ĭ				List
Bottom Pins	Ĭ.				List
Load/Save 📃	Edit Att	ributes 📃	Edit Labels	Edit	Properties 📃

Drawing 15: Symbol options

- Symbol editing, step 4 [Drawing 16]. You can rearrange pins and other macro objects in case you dont like defaults



Drawing 16: Symbol editing

Exporting circuit (EDIF 200) to Turbo Tester

Locate window named 'icfb' and open menu as shown on [Drawing 17].

File Tools Options	Technology File HIT-Kit utilities	Help	1	
^I New Den	LL e check the file edifout.log for more information			
Export Refresh Make Read Only Close Data Defragment Data Exit	EDIF 200 EDIF 300 PRFlatten CDL DEF			
I	Stream Applicon CIF Router			
mouse L: mouseAddPt	t() M: schHiMousePopUp() R: Rotate 90			
Use the options form	to supply the wire names.			

Drawing 17: Exporting desing, step 1

A large dialog window appears [Drawing 18]. Filling it takes some steps:

- select circuit to be exported. This is done via 'Browse' button opening 'Library Manager' window where you can select your design (and schematic view!)
- specify 'HRDLIB' for fields 'External Libraries' and 'Stop Cell Expansion File'. The latter is most
 important as this wont let transistor level data into your export (Turbo Tester importer cannot
 handle that).
- specify design name. Turbo Tester importer need it, although leaving it blank wont otherwise affect export process in any way.
- specify EDIF output file. Your circuit will be written there. When importing to Turbo Tester, this file name is used for resulting AGM file.
- set 'Output format' to 'Netlist' as we need the circuit only.
- set 'NetlistTranslationMode' to 'Flat', it will flatten (ie. unwrap) all macros.

ОК	Cancel	Defaults	Apply		Help				
Template	File	-	02/ic446/1	tools.sun4v/dfII/samples/xlUI/edifOut.il					
		l	oad Save						
Design		I	Browse						
Run Direc	tory	ŀ	Ĭ.						
Library N	ame	1	testį						
Cell Name	•	1	testcell						
View Nan	ne	\$	schematic						
External I	libraries	Ι	IRDL IB						
Design Na	ame	[testcell						
User-Def	ined SKIL	L File							
Hierarchy	File	Ĭ							
Stop Cell	Expansior	n File 🛛 I	HRDLIE						
Output Fi	le	1	testcell.edif						
Technolog	jy File		default.tf						
Output Cl	DF Data	Γ							
ReplaceB	undleWith	Array (TRUE C	FALSE					
Output Fo	ormat) Schemati	ic 💿 Netlist					
Generate	Scalar El	DIF (FALSE						
) INVE	expand All Objects					
			Ŏ	xpand All Objects Except Ports					
Inherited	Connectio	ns () Use Defa) Interpret	ult Value (Ignore Expressions) Expressions					
NetlistTra	unslationM	lode () Hierarchi	cal 🖲 Flat					
Skip Dupl	icate Insta	ance Nan	ne Check						
Flatten R	un Directo	iry	Ĭ						
Ripper Lik	orary Nam	ie I							
Flatten Ri Ripper Lik	un Directo orary Nam	iry ie	<u>¥</u>						

Drawing 18: Exporting, step 2

Importing EDIF to Turbo Tester

Turbo Tester has special import library for 'HRDLIB' called 'ams.lib'. This library defines all HRDLIB elements (at least it should). Issue following command for the import:

'import -tool cadence <edif file name> ams.lib'.