Understanding Boundary Scan

Student Code: _____

Student Name: _____

Assignment no.: _____

Getting started

1. Start the Trainer 1149 (type '1149')
2. Open "BS_Exercises" project and select "**Board_#.nl**" file from *Netlists* folder. (**#** - reflects assignment number)

1. TAP Controller and TAP State Diagram

Using the TAP state diagram, TMS, TDI, TDO do the following:

1. Fill the following table with appropriate instruction names used with **D#** component

Instruction Code:	000	001	010	011	100	101	110	111
Instruction Name:								

Hint: use BSDL file of selected IC to find the Instruction names, if name is missing – simulate the instruction code using the TAP state diagram, TMS, TDI, TDO and TCK. D#.BSD files are located in *Components* folder.

2. Read IDCODE & USERCODE contents from **D#** IC and record them:

IDCODE 32 bits	Bin	
	Hex	
USERCODE 32 bits	Bin	
	Hex	

Compare obtained binary code with the value in .BSD file of the IC and hexadecimal code with the value displayed in the chip graphical view.

3. Shift BYPASS, BYPASS, SAMPLE/PRELOAD instructions to chips SN74BCT8244A, D#, SN74BCT8244A, correspondingly

4. Use *BS Register* to control the output LEDs on *BufferOUT* IC. The task is to get the binary representation of your assignment number (two last decimal digits) being displayed on the LEDs. Example: assignment no. is 23_{DEC}, which is 10111_{BIN}, and hence LEDs are 00010111. Use SAMPLE/PRELOAD in *BufferOUT* to shift in necessary data and EXTEST to drive the LEDs.

IR sequence	
DR sequence	
IR sequence	

5. Answer the question: what is the minimum number of clock cycles that is enough to return to the *Test-Logic-Reset* state from any random state when keeping TMS signal high?

2. Cluster Test

1. Switch to debug mode.
2. Using BS registers, apply stimuli to the cluster inputs and measure cluster output responses in order to determine the functionality of the cluster. Use the following sequence of instructions:
3. Define the first test stimulus and apply SAMPLE/PRELOAD, BYPASS, SAMPLE/PRELOAD instructions to chips SN74BCT8244A, D#, SN74BCT8244A, correspondingly.
4. Define the second test stimulus and apply EXTEST, BYPASS, SAMPLE/PRELOAD instructions.
5. Repeat with EXTEST, BYPASS, EXTEST instructions until you know the Boolean function of the cluster. *Remember that output responses for current data are ready at the next test cycle!*
6. Fill in the truth table of the cluster and decide which logic gates(s) are inside the cluster.

A	B	Y
0	0	
0	1	
1	0	
1	1	

Draw cluster's schematic here!

7. Compose tests to detect all stuck-at faults (SAF) for the cluster and apply them

	IC	Instruction	Test Data	Fault detection
Test 1	IC 1			
	IC 2			
	IC 3			
Test 2	IC 1			
	IC 2			
	IC 3			
Test 3	IC 1			
	IC 2			
	IC 3			

3. Interconnect Testing and Fault Diagnosis

Using the Debug Mode do the following:

1. Select "TwoChips" board configuration
2. Select Diagnostics -> Insert Fault -> Random Fault
3. Generate test patterns both for opens and shorts (True/Complement Counting Code)
4. Apply them one by one and record the results (remember that data is captured on the next cycle)
5. Make diagnosis and decide which fault has been inserted

Interconnect nets	Test patterns	Output responses	Pass/Fail
Net0			
Net1			
Net2			
Net3			
Net4			
Net5			
Net6			
Net7			
Pass/Fail			

Fault diagnosis:_____