IR Remote Control and LCD Display

Task:

Using DE2-115 board read scan codes of the IR remote control keys and output them on the LCD display. Refer to DE2-115 board manual for pin numbers.

IR data transmission

Transmission of IR data is carried out via a single-wire bus. The format of a standard data frame is shown in Figure 1. The frame begins with a singe bit start code. It is followed by a 16-bit custom core that identified the transmitting device. Next comes an 8-bit scan code of the pressed key and its inverted versions. The 1-bit stop code closes the data frame. If the key remains pressed, then the next data frame contains only start and stop codes.

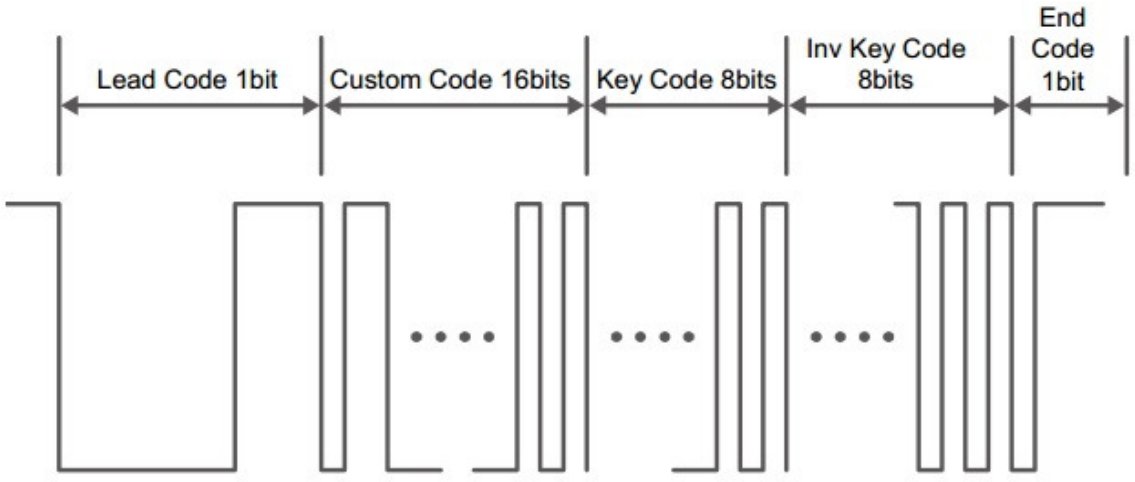

Figure 1: Format of the IR data frame

As there are no additional synchronization signals the only way to interpret the incoming data stream is to follow the timing of pulses. The start bit begins with a 9ms gap followed by a 4,5ms pulse (2.25ms in the subsequent frame if the key remains pressed). The data gaps are approximately 600us long, while the pulse width depends on the encoded value: 600us for ‘zero’ and 1600us for ‘one’. The gap in the stop code is 600us long, while the

pulse width depends on the remaining time in the frame time slot (the whole frame should last about 108ms). Note that the provided timing values are highly approximate (plus they may depend on other environmental conditions like the distance between transmitter and receiver, lighting, etc.). Thus some experimentation may be required for fine-tuning,

LCD Display

LCD display is a very handy tool for showing information, debugging, etc. As a rule, LCDs require fewer connections than LED displays and use less power, but they are controlled in a much more complex way. Eight pins form data bus (DB7-DB0). Enable pin (E), register select pin (RS), read/write select pin (R/W) are used for control. Typically, LCD is equipped with a controller, which internally does all the functions using commands sent by the user designed Finite State Machine or processor. It has two externally controlled 8-bit registers – instruction register (IR) and data register (DR). IR stores instructions and address information, DR – data to be written or read. Write and read operation is selected via R/W input signal, register is selected using RS input signal. Table 1 lists all available IR and DR operations.

Table 1: IR and DR operations

RS	R/W	Operation
0	0	Instruction is written to IR
0	1	Busy flag (DB7) and address counter (AC) value (DB6-DB0) are read
1	0	Write data from DR to DDRAM or CGRAM
1	1	Read data from DDRAM or CGRAM to DR

Note that IR register can only be written. When IR is selected and R/W input is High (indicating read operation) busy flag and address counter value are read instead. Busy flag is set High while internal operation is being performed, so the next instruction will not be accepted. Thus, new instruction must be sent only after busy flag is cleared (set to Low). Many prefer to use appropriate delays instead of polling, though.

Address counter (AC) holds addresses to both DDRAM and CGRAM. Memory selection is determined by the instruction. Note that after writing to (reading from) DDRAM or CGRAM, AC is automatically incremented or decremented by one (direction is selected using appropriate instruction).

Home position

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

After shift left

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

After shift right

4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

Figure 2: 16x1 display visible DDRAM area (addresses are presented in HEX format)

Home position

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

After shift left

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

After shift right

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

Figure 3: 16x2 display visible DDRAM area (addresses are presented in HEX format)

The abbreviations DDRAM and CGRAM refer to the two types of memory used by LCD module controller. DDRAM stands for display data RAM. It stores eighty 8-bit character codes (although only 16 or 32 characters can be displayed at once). With shift instruction the viewable part of DDRAM can be altered. Figure 2 and Figure 3 illustrate relationships between DDRAM addresses and the visible area of the LCD module for different display modes.

Figure 4: A00 model character generator patterns

Note that when in 16x2 mode the first line is represented by DDRAM address range starting from 00h down to 27h (forty characters in total), but the second line starts from 40h and ends with address 67h (also forty characters in total).

Values stored in DDRAM are actually addresses for the character generator, which stores 5x7 dot and 5x10 dot character patterns. It consists of CGRAM and CGROM. CGROM holds predefined character patterns, while CGRAM can be programmed to store custom ones (either eight 5x7 dot or four 5x10 dot characters for LCD module provided with UP3 board). Figure 4 illustrates A00 model character generator patterns.

The leftmost column in Figure 4 represents CGRAM. CGRAM custom character pattern is programmed line by line. Note that only five least significant bits would be represented in character pattern. It is recommended to write empty lines as well as on power-up CGRAM may not be totally empty. Note that custom characters get duplicated. For example, codes 00h and 08h represent one and the same custom character pattern.

Table 2. LCD module instructions

Instruction	D7	D6	D5	D4	D3	D2	D1	D0
Clear display	0	0	0	0	0	0	0	1
Cursor at home	0	0	0	0	0	0	1	---*
Entry mode set	0	0	0	0	0	1	I/D	S
Display control	0	0	0	0	1	D	C	B
Cursor or display shift	0	0	0	1	S/C	R/L	---	---
Function set	0	0	1	DL	N	F	---	---
CGRAM address set	0	1	ADDRESS					
DDRAM address set	1	ADDRESS						

*) “---“ denotes don’t care value

LCD module uses eight 8-bit wide instructions. These commands are differentiated by the leftmost non-zero bit. Bits to the right of the instruction bit represent additional parameters. Table 2 lists all available instructions.

Clear display instruction writes 20h (space character code) to all DDRAM addresses and writes 00h to AC, cursor is returned to home position and entry mode direction is set to increment. Cursor at home instruction basically does the same, but DDRAM content and entry mode direction are left unchanged.

Entry mode instruction sets the way characters are written and read. I/D parameter defines whether AC value would increment (when set to High) or decrement (when set to Low) after data is written to or read from either DDRAM or CGRAM. With S bit enabled (set to High) writing data to DDRAM will shift visible memory area right or left, visually leaving cursor at the same position. I/D bit defines shift direction (left when High, right when Low). When S bit is disabled (set to Low) visible memory area position is not changed, thus cursor would visually move to the next position.

Display control instruction is used to manage LCD visual appearance. D bit turns display ON/OFF (DDRAM content remains unchanged), C bit makes cursor visible or hides it and B bit defines whether the character at the cursor position will blink or not. Setting parameter High enables corresponding feature, Low value disables it. Note that cursor or blinking position is determined by the address stored in AC. If AC stores CGRAM address, then cursor or blinking would occur at the wrong place.

Cursor or display shift instruction either moves cursor one position or shifts entire display left or right. S/C bit selects cursor (Low value) or display shift (High value), R/L determines direction (left when Low, right when High). Note that in two-line mode cursor jumps to the second line after the 40th character of the first line.

Function set instruction defines some hardware aspects of display. DL bit selects either 8-bit (High value) or 4-bit (Low value) interface. When using 4-bit interface only four data

bus lines are active (DB7-DB4), the rest is disabled. Firstly, four high order bits of data are transferred, then four remaining low order bits. N bit sets the number of display lines (one line when Low, two lines when High). F bit defines character size (5x10 dots when High, 5x7 dots when Low).

CGRAM address set instruction loads AC with the value specified in the address field and causes subsequent data to be stored in the character generator RAM. DDRAM address set instruction does exactly the same, but this time the display data RAM is selected.

On power up LCD module performs internal reset itself. However, if power supply problems occur, internal reset circuit would not function correctly. It may be necessary to provide initialization by instruction. The initialization sequence is as follows:

- POWER ON
- 15 ms delay
- Function Set
- 4.1 ms delay
- Function Set
- 100 μs delay
- Function Set
- 5 ms delay
- Function Set
- Display OFF
- Display ON
- Entry Mode Set