On reusability of verification assertions for testing

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Abstract

Assertions have proven to be an effective mechanism to improve quality and to speed-up simulation-based design verification. They are created and embedded to the simulatable design description by the designer, the person with the deepest knowledge about the desired functionality and its real implementation. In this paper we propose to reuse this valuable information during the design manufacturing testing phase to increase the test quality and efficiency. The paper considers different types of design properties created for verification such as environmental assumptions and internal signal assertions. The reusable information is proposed to be applied for test pattern generation, embedded test observability improvement and DfT (design for testability) enhancement.

1. Introduction

As the digital hardware complexity grows very fast, its functional verification, meant to ensure that design fulfills the given specifications, is extremely important step in the whole development flow. Simulation-based (dynamic) and formal (static) approaches are two major types of verification. Both of them can imply assertions to improve the quality and speed-up the verification process. However from now on we will consider mainly assertions and other types of properties created for simulation-based verification.

The assertions are created by designer and contain a very valuable knowledge about the design’s functionality and structure. During the verification phase they are simulated together with the design and help to discover design’s incorrect implementation faster and more efficiently ([1],[2],[3],[4]). Further, the assertions are removed from the design’s synthesizable version.

However the correct implementation of the design’s given specification does not guarantee that the product will get to the customer fault-free. The manufacturing phase should be followed by an appropriate testing as well. The task of the test preparation can be aided by

![Figure 1. ASIC development flow](image-url)
Self-Test quality improvement with assertions. Section 4 proposes a DfT technique applying assertions for test points insertion. Section 5 concludes the paper.

2. Assumption-based Test Generation

A part of today manufactured ASICs contains embedded during DfT scan-chains that increase observability and controllability of the circuits under test (CUT) by providing an access to the internal registers. This method allows reaching high fault coverage, however it results in over-testing of the core (see e.g. [16]). In other words, it covers faults that could never influence the functional behavior of the circuit thus reducing the yield. From another hand, it has been shown that non-scan testing based on pseudorandom test sequences can be highly feasible for several types of designs (such as crypto cores as it was proven in [17]). Finally, not all the circuits may have the embedded scan. The ideas proposed in this paper consider non-scan sequential circuits. However they can be partially applied to scan circuits as well.

The notion of test cubes is applied for test set representation when several bits in the test vectors contain “don’t care” values X (See Fig. 2). These bits can be assigned to the normal binary values “1” or “0” whether based on some rules or just randomly. The “X”-s add the 3rd dimension to the fully determined 2-dimensional test set.

In case if the test engineer has no prior information about the CUT’s input data dependencies (assumptions) he has to start with a test set filled with all X-s (an empty set). The assumptions provide information how to assign a part of the bits in the test cube which increases the final test quality and eases the test generation process. For example if an assumption provides us information that some particular input (pin) of the CUT is its RESET signal, then the test engineer may decide to set its value to “1” only once in some sequence of cycles. The assumptions may be much more complex and origin from a design specification and its implementation (design) phase.

Both the assumptions (sometimes referred also as environmental constraints) and assertions are design properties. The first ones contain information about the design’s environment and therefore its expected inputs dependencies while the second ones describe the dependencies of the design’s internal signals and outputs [23]. Usually both the assumptions and assertions are described in one of the property description languages such as SVA (System Verilog Assertions, [20]) or PSL (Property Specification Language, IEEE 1850 standard, [21],[22],[23]).

The assumptions can be described explicitly by the designer or implicitly follow from some of the given assertions of the connected designs or design cores. The latter case is shown in Figure 3 and known as assumption-assertion dualism [24]. This method allows obtaining a wider set of assumptions.

The main difference of the proposed approach from the one described in [6],[7] is the formal source and format of the assumptions.
enhancement. The Built-In Self-Test (BIST) has been proven to be an efficient approach for manufacturing testing. However in case of non-scan circuits its main bottleneck is observability.

A method for verification assertions synthesis to hardware assertion checkers embedded to the circuits for on-line testing is proposed by Riazati, Navabi et al in [8],[9] and by Boule in [11]. A number of approaches for assertions checkers creation meant for prototype verification/ validation by emulation (a development flow phase standing before mass-production), such as [2],[12],[13],[14],[15] can be extended for this purpose. The most widely known commercial tool for usual assertions conversion to their synthesizable form is FoCs from IBM [18],[19].

We propose to apply the verification assertions in the form of hardware assertion checkers for BIST observability enhancement. They could act as separate observers in BIST response analyzer architecture. The second application for them is to be a part of response analyzer controller guiding the analyzer when to check and when to stay in Silence Mode.

4. Assertion-based DfT

The two main components of CUT’s testability are observability and controllability. The second one can be significantly improved during DfT phase. These improvements usually include minor rearrangements inside the design or addition of an extra logic (for example scan-chains as it was mentioned in Section 2).

One of the DfT techniques is “test points insertion”, when an additional auxiliary input pin is routed to an internal net of the CUT. The main drawback of this technique is hardware area overhead, and what makes it even more significant input pins overhead that are very costly. Therefore, only the nets providing good controllability coverage should be chosen. The identification of such nets is a very complex task, usually solved by heuristics.

We propose to use for test points the nets corresponding to the signals (operands) form assertions (Fig. 4).

The good candidates for test points locations are the nets with hard-to-test faults, due to very low controllability. The other intent for test point insertion would be a fan-out that provides at once a good controllability to a set of middle-level controllability places. Such a test point would shorten the test length.

The both criteria can be usually satisfied by normal assertions, because the assertions reflect the designer’s conception of the most significant cornerstones of the design.

Test points insertion to the sequential circuits may lead at some extend to the same drawback of over-testing as in case of scan-chains insertion mentioned in Section 2.

Experimental results are needed to estimate the efficiency of the proposed approaches. Their implementation is left for the future work.

5. Conclusions

This is an overview paper focusing on the reusability aspects of simulation-based verification assertions for manufacturing testing. The ideas presented here propose an extended reusability of the valuable information about CUT’s (circuit under test) properties created during its design phase for a more efficient test development.

The paper considers different types of design properties created for verification such as environmental assumptions and internal signal assertions. The reusable information is proposed to be applied for test pattern generation, embedded test observability improvement and DfT (design for testability) enhancement.

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Figure 4. Assertions for test points insertion
References


