Design for Test and Low Power Test

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Tutorial flow

• Design for Testability
• Tools for DTF
• Low Power Testing
### ATPG Design Rules

- No combinational feedback / no sequential elements made from combinational feedback
- No non-gate-level logic / no transistor level design
- No non-deterministic logic
- No clock signals used as data / no data used as clock
- No free-running internal clocks / no internally generated clocks during scan
- No use of both edges of a clock

[Crouch A., L., *Design for Test*] 3

### ATPG Design Rules

- No asynchronous sequential logic
- No gated clocks to sequential elements

**Exceptions:**
- Asynchronous set / reset elements
- Gated clocks
- Transistor construct

[Crouch A., L., *Design for Test*] 4
Scan-Based Design Rules

- No asynchronous set/reset/hold in synchronous elements with asynchronous function or with higher priority than scan operation
- No synchronous latches
- No cross-coupled gates
- No reset dependency during scan
- No internal nodes that support other logic than 1/0

(cont…)

[Crouch A., L., Design for Test]

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Scan-Based Design Rules

- No registered test mode logic
- No test mode select logic that can be changed during scan operation by scan operation
- No self-timed logic
- No asynchronous pin-to-pin logic
- No dynamic logic (pre-charge, pullup…)
- no non-constrained memory logic

(cont…)

[Crouch A., L., Design for Test]

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Scan-Based Design Rules

- No multiple clock domain within a single scan domain
- No derived clocks (negedge / freq. division)
- No gated clocks
- No data inversion between cells
- No long scan chains (up to 150 bits)
- No unbalanced scan chains (the same length)
- (etc…)

[Design for Test] by Crouch A., L.

Design for Testability

- **Structured Design**
  - Serial Methods (LSSD, Scan Path, Scan/Set Logic)
  - Parallel Methods (RAS)
- **Boundary Scan**
- **Ad-Hoc Methods**
  - Partitioning, Bus Architecture, Signature Analysis
• Structured Design
  • Serial Methods (LSSD, Scan Path, ScanSet Logic)
  • Parallel Methods (RAS)
• Boundary Scan
• Ad-Hoc Methods
  • Partitioning, Bus Architecture, Signature Analysis
Design for Testability

- **Structured Design**
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  - **Parallel Methods (RAS)**
- Boundary Scan
- Ad-Hoc Methods
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[Williams T., W., Parker H., P., Design for Testability – A Survey]
Design for Testability

- Structured Design
  - Serial Methods (LSSD, Scan Path, ScanSet Logic)
  - Parallel Methods (RAS)
- **Boundary Scan**
- Ad-Hoc Methods
  - Partitioning, Bus Architecture, Signature Analysis
Boundary Scan

SO (Serial Output)

NI (Normal Input)

OBSERVE

CONTROL

TEST/DATA MUX

SCAN LATCH/FLOP

UPDATE LATCH/FLOP

NO (Normal Output)

SI (Serial Input)

Tools for DFT

- Mentor Graphics
  - DFTAdvisor
  - Flextest, Fastscan, LBIST, MBIST

- Cadence
  - Ambit

- Synopsys
  - Design_Analyzer, Design_Vision
**DFTAdvisor**
DFTAdvisor is a testability analysis and test synthesis tool. DFTAdvisor's comprehensive rules checking engine ensures that testability issues are caught early in the design flow.

[D www.mentor.com](http://www.mentor.com)

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**FlexTest**
FlexTest is the ideal solution for test pattern generation when you need to optimize test coverage for non-scan, partial-scan or full-scan designs.

[D www.mentor.com](http://www.mentor.com)
FastScan
FastScan, the industry's premier automatic test pattern generation tool, creates high-quality tests for ASICs and ICs using full or structured partial scan.

BSDArchitect
BSDArchitect automatically generates IEEE 1149.1 compliant boundary-scan logic.
**MBISTArchitect** is a tool that adds Built In Self Test (BIST) to memories. Though it may be applied to a variety of memory types, the most common applications are embedded SRAM and ROM.

**LBISTArchitect** performs circuit analysis and hardware generation for an embedded structural test methodology, which eliminates the need for external pattern sets. This method of IC testing is often called Built-in-Self-Test (BIST).

**DFTInsight**'s graphical debugging environment makes it easy to analyze your ASIC or IC testability problems. Invoked within either DFTAdvisor, FastScan or FlexTest, DFTInsight generates a schematic view to display information, making it easier to isolate and correct testability problems.

[www.mentor.com]

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**BuildGates**

BuildGates® Synthesis enables rapid synthesis of multimillion-gate designs with superior results. It delivers dramatic performance and productivity benefits over conventional synthesis tools, yielding enhanced quality-of-results (QOR) with less manual intervention.

[www.cadence.com]
Design Analyzer
Design Analyzer is a powerful analysis tool that gives you synthesis control, design management, and design analysis in a graphical environment.

[www.synopsys.com]

DesignVision
DesignVision is the new GUI for DC, enables intuitive and easy-to-use visual analysis of designs. It allows users to obtain an overview of the timing of their design, visualize the details of timing paths, and write custom tcl scripts that interact with the GUI. Design Vision also offers synthesis control and design management, allowing users to perform various design set-up and analysis functions interactively.

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[www.synopsys.com]
Partitioning

Ad-Hoc Methods

- Bus Architecture
- Signature Analysis
- Test Points
• Hardware Optimization
• TPG structure

Novak O., *Pseudorandom, Weighted Random and Pseudoexhaustive Test Patterns Generated in Universal Cellular Automata*

Ravikumar C., P., *Evaluating BIST Architectures for Low Power*
Low Power Testing

• Hardware Optimization
  • TPG structure
  • Multiple Scan Chains

Nicolici N., Al-Hashimi B., M., Scan Latch Partitioning into Multiple Scan Chains for Power Minimization in Full Scan

Multiple Scan Chain

Nicolici N., Al-Hashimi B., M., Scan Latch Partitioning into Multiple Scan Chains for Power Minimization in Full Scan
Low Power Testing

- Hardware Optimization
  - TPG structure
  - Multiple Scan Chains
  - Cells with Reduced Output Activity

Gerstendoerfer S., Wunderlich H.-J., *Minimized Power Consumption for Scan-Based BIST*

Reduced Output Activity

Gerstendoerfer S., Wunderlich H.-J., *Minimized Power Consumption for Scan-Based BIST*
Low Power Testing

- Hardware Optimization
  - TPG structure
  - Multiple Scan Chains
  - Cells with Reduced Output Activity
  - Dual Speed

Wang S., Gupta S., K., *DS-LFSR – A New BIST TPG for Low Heat Dissipation*
Low Power Testing

- Hardware Optimization
  - TPG structure
  - Multiple Scan Chains
  - Cells with Reduced Output Activity
  - Dual Speed
  - Test Vector Inhibiting Technique (cont...)

Girard P., a col., *A Test Vector Inhibiting Technique for Low Energy BIST Design*

Test Vector Inhibiting

[Diagram showing a LFSR, Decoding Logic, D-Q flip-flops, and a Circuit Under Test]

Girard P., a col., *A Test Vector Inhibiting Technique for Low Energy BIST Design*
Low Power Testing

- Hardware Optimization (cont.)
- Filtering Non-Detecting Vectors

Filtering Vectors

Manich S., a col., *Low Power BIST by Filtering Non-Detecting Vectors*
Low Power Testing

- Hardware Optimization (cont..)
  - Filtering Non-Detecting Vectors
  - Circuit Partitioning

Girard P., a col., *Circuit Partitioning for Low Power BIST Design with Minimized Peak Power Consumption* 43

Circuit Partitioning

(a) Circuit Partitioning

(b) Circuit Partitioning

Girard P., a col., *Circuit Partitioning for Low Power BIST Design with Minimized Peak Power Consumption* 44
• Hardware Optimization (cont..)
  • Filtering Non-Detecting Vectors
  • Circuit Partitioning
  • Optimal Vector Selection

Corno F., a col., *Optimal Vector Selection for Low Power BIST*
Low Power Testing

- Hardware Optimization (cont.)
  - Filtering Non-Detecting Vectors
  - Circuit Partitioning
  - Optimal Vector Selection
  - etc.

SoC

[Crouch A., L., Design for Test]
• Reuse Cores
  • Soft (HDL, RTL)
  • Firm (GLM)
  • Hard (GDSII)

[Crouch A., L., *Design for Test*]

• Chip Pin Interface
• Reuse Core Unit(s)
• IEEE 1149.x Architecture
• Embedded clock source
• Embedded Memory Array(s)
• Non-Core / User-Defined Chip Logic
• Chip-Level Test Control Unit
• Overall test !!
SoC – Core Reuse

Test Access to the Core Interface

• Soft / Firm

[Crouch A., L., Design for Test]
SoC – Core Reuse

Test Access to the Core Interface

- Soft / Firm

- Hard
  - Do Nothing
  - Direct Access

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SoC – Core Reuse

Test Access to the Core Interface

- Soft / Firm

- Hard
  - Do Nothing
  - Direct Access
  - Slow JTAG
  - BIST

[Crouch A., L., Design for Test]
SoC – Core Reuse

Test Access to the Core Interface

- Soft / Firm

- Hard
  - Do Nothing
  - Direct Access
  - Slow JTAG
  - BIST
  - Stored Pattern Test
  - At-Speed Scan

[Crouch A., L., Design for Test]

Wrappers

Wrappers

(Test Ring/Test Collar/Test Wrapper/Boundary Ring/etc.)

Primary purpose: *allow “test-in-isolation”*

- as Signal Reduction Element
- as Frequency Interface
- as a Virtual Test Socket
  - Add-on / Slice / Partition-Cell
  - Shared / Merged / Registered

[Crouch A., L., Design for Test]
Definitions of Chip-Level DFT Integration:

- Non-Mergeable
- Mergeable
- Hard Core
- Soft Core
- Firm Core
- Test-In-Isolation

[Crouch A., L., *Design for Test*]