**eVikings II**

**Establishment of the Virtual Centre of Excellence for IST RTD in Estonia**

FP5 IST accompanying measures project IST-2001-37592

Deliverable D4.4:

# Semiconductor Technology, Design and Test Roadmap

*Jaan Raik, Raimund Ubar*

Department of Computer Engineering
Tallinn Technical University, Estonia


Tallinn
October 2003

## Table of contents

# 1. Introduction

In 1992, The National Technology Roadmap for Semiconductors was published in an effort to identify the challenges facing the semiconductor industry in maintaining its previous rate of growth. Since then, new roadmaps have been presented every 2-3 years, the consortium has grown and become international. While in the first roadmaps only technology-related issues were present, later design and also test topics have joined in.

The most important work we refer to in current report is The International Technology Roadmap for Semiconductors (ITRS), more precisely the 2001 edition [1], which foresees the technological challenges and needs facing the semiconductor industry over the next 15 years and its 2002 update [2]. The main goal of this report is to give an overview of the predicted trends in microelectronic systems design, technology and test according to the leading roadmaps.

The report is organized as follows. We start with discussing the main developments in semiconductor industry in general. Then we talk about the system drivers for design focusing on future issues for microprocessors. We continue with naming the main challenges in the design area and moving on to the trends in test methods, tools and the Automatic Test Equipment (ATE). Finally, we are going to assess what would be the impact of the changes predicted by the roadmap to the Estonian research community and industry in the microelectronics field. Physical and technology related issues are considered throughout the report as the evolving background to the future developments of system design and test.

# 2. Summary of trends

Already for more than 40 years the evolution of semiconductor devices has been following the Moore's law, which states that their most important characteristics are improved four times every three years. The most significant implication for society is the 25-30 % annually decreasing cost per function, which has significantly improved quality of life in terms of proliferation of computers, telecommunication and consumer electronics. However, it is an immense challenge for the semiconductor industry to keep up with the Moore's law and the rate of drop in function cost to allow 15 percent annual growth of the market for integrated circuits. In order to address this challenge industry cooperation in the form of parterships and consortia has emerged to promote development of roadmaps as the "best current estimates" of its R&D needs for years to come.

In [4], the main future issues concerning semiconductor devices are divided into 3 domains: scaling, speed and cost. Let us briefly consider each of the mentioned domains.

**Scaling**
Dynamic random access memory (DRAM) and microprocessing unit (MPU) models are dependent on achieving agressive design and process improvement targets. If those targets slip, there will be a pressure to either print larger chip sizes or to the increase on-chip functionality slower than the Moore's law indicates. Both of these consequences will have a negative impact upon cost-per-function reduction levels – the classical measure of semiconductor industry's productivity, improvement and competitiveness [4].

**Speed**
Moore's law does not apply merely to the amount of functions that can be accomodated to the chip die but concerns also other important characteristics like processing speed. In the case of MPUs, processor instructions per second have also historically doubled every 1.5 to 2 years [4]. Increase in the most important measure for MPU's processing power, millions of instructions per second (MIPS), can be achieved by a combination of technology performance (clock frequency) multiplied by architectural performance (instructions per clock cycle). However, as the architectural advances (e.g. pipelining) become fully exploited the growth in processing speed will become almost directly dependent on acceleration in the clock rate (See Table 1).

In general, signal propagation becomes more difficult due to increased capacitive and inductive coupling, which degrades edge rates and causes both timing uncertainty and potential logic errors. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be required for adequate suppression of parasitic effects caused by the package [4].

**Cost**
The ability to reduce the cost per function by 25 to 30 percent each year is a unique feature of the semiconductor industry and is the fundamental engine behind its growth. In support of this cost reduction, R&D and manufacturing require a continuously increasing financial investment. Even on a per-factory basis, the capital cost of manufacturing continues to escalate.

However, the 2001 ITRS roadmap [1] predicts that the number of transistors per MPU chip can double only every three years after 2001. Even though the rate of increase in on-chip complexity could slow in the future, the number of functions per chip will continue to grow. Increased chip functions drive for example an increase of test-method complexity, which in the past resulted in nonlinear cost increases to manufacturing test in capital for additional ATE (automated test equipment) hardware and longer device test times [4]. Table 1 reflects the main trends in scaling, cost and power according to the ITRS roadmap for 2003-2016.

Table 1. Trends in scaling, cost and power for 2003-2016.

| Production year | 2003 | 2004 | 2005 | 2006 | 2007 | 2010 | 2013 | 2016 |
|---|---|---|---|---|---|---|---|---|
| Chip performance | | | | | | | | |
| DRAM half-pitch | 100 | 90 | 80 | 70 | 65 | 45 | 32 | 22 |
| MPU/ASIC half-pitch | 107 | 90 | 80 | 70 | 65 | 45 | 32 | 22 |
| MPU printed gate length | 65 | 53 | 45 | 40 | 35 | 25 | 18 | 13 |
| MPU physical gate length | 45 | 37 | 32 | 28 | 25 | 18 | 13 | 9 |
| On-chip local clock (MHz) | 3,088 | 3,990 | 5,173 | 5,631 | 6,739 | 11,51 | 19,35 | 28,75 |
| Max. number wiring levels | 8 | 8 | 9 | 9 | 9 | 10 | 10 | 10 |
| Cost per function (µcents) | | | | | | | | |
| DRAM (cost/bit) | 3.8 | 2.7 | 1.9 | 1.4 | 0.96 | 0.34 | 0.12 | 0.042 |
| CP-MPU (cost/transistor) | 53 | 38 | 27 | 19 | 13.3 | 4.71 | 1.66 | 0.590 |
| HP-MPU (cost/transistor) | 49 | 34 | 24 | 17 | 12 | 4.31 | 1.52 | 0.540 |
| Test cost (k$/pin) | | | | | | | | |
| Volume tester cost per high-frequency signal pin (HP-ASIC) - maximum | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 4.0 | 4.0 | 4.0 |
| Volume tester cost per high-frequency signal pin (HP-ASIC) - minimum | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 2.0 | 3.0 | 4.0 |
| Volume tester (CP-MPU) | 6.0 | 5.5 | 5.0 | 4.5 | 4.0 | 4.0 | 2.0 | 1.5 |
| Power supply voltage (V) | | | | | | | | |
| Vdd (high performance) | 1.0 | 1.0 | 0.9 | 0.9 | 0.7 | 0.6 | 0.5 | 0.4 |
| Vdd (low operating power, high Vdd transistors) | 1.1 | 1.1 | 1.0 | 1.0 | 0.9 | 0.8 | 0.7 | 0.6 |
| Vdd (low standby power, high Vdd transistors) | 1.2 | 1.2 | 1.2 | 1.2 | 1.1 | 1.1 | 1.1 | 1.1 |
| Allowable max. power (W) | | | | | | | | |
| High-perform. w heatsink | 150 | 160 | 170 | 180 | 190 | 218 | 251 | 288 |
| Cost-performance | 81 | 85 | 92 | 98 | 104 | 120 | 138 | 158 |
| Battery (handheld) | 2.8 | 3.2 | 3.2 | 3.5 | 3.5 | 3.0 | 3.0 | 3.0 |

## 3. System drivers for design

Let us take a closer look in possible future issues concerning the design process of the semiconductor devices according to the leading roadmaps. The ITRS 2001 roadmap [1] focusses on three main system drivers: high-volume custom – microprocessor (MPU), analog/mixed-signal (not considered in current report) and system-on-chip (See Section 4). A fourth system driver, high-volume custom – memory (DRAM) that has been present in previous editions is neglected due to its well understood commodity nature. Previous editions of the ITRS roadmaps have included application-specific integrated circuit (ASIC) driver instead of SOC. While somewhat similar, the main difference between the two is that SoCs emphasize reusing intellectual property (IP) to improve productivity. In addition, SoC integration potentially encompasses heterogeneous technologies.

High-volume custom MPUs implement the most innovative and agressive design styles and manufacturing technologies. These high-volume parts drive the developers to introduce changes to the manufacturing flow, create new design styles and supporting tools and uncover subtle circuit issues. Thus, while developing custom MPU designs is extremely labor intensive, they offer new design and fabrication technology and new automation methods that the entire industry utilizes [4].

According to the "MPU Evolution" section of the ITRS 2001 roadmap [1] the key issues for the future developments of the traditional MPU are related to design productivity, power management, multi-core organization, I/O bandwidth and circuit and process technology. Let us consider each of these key contexts.

**Design productivity**
The complexity and cost of design and verification of MPU products has rapidly increased to the point, where thousands of engineer-years (and a design team of hundreds) are devoted to a single design, yet processors reach market with hundreds of bugs [1].

**Power management**
MPUs would not be able to continue using existing circuit and architecture techniques since by doing that they would exceed package power limits by a factor of more than 25 times by the year 2015 [4]. Alternatively, MPU logic content and/or logic activity would need to decrease to match the package constraints [1].

Another important trend: power efficiencies for direct-mapped hardware are up to four orders of magnitude greater than for general-purpose MPUs, and this gap is increasing. As a result, traditional processing cores will face competition from application-specific or reconfigurable processing engines in the future [4].

**I/O bandwidth**
In MPU systems, I/O pins mainly connect to both high-level cache memory and main-system memory. Increased processor performance has been pushing I/O bandwidth requirements. Caches traditionally use the highest-bandwidth port, but recent designs integrate the memory controller on the processor die to reduce memory latency. These direct memory interfaces require more I/O bandwidth than the cache interface [1].

Many designs replace the system bus with high-speed point-to-point interfaces that require much faster I/O design, exceeding gigabit-per-second rates. However, integrating a large number of these I/Os on a single chip presents challenges for design, test and packaging [1].

**Circuit and process technology**
The ITRS roadmap warns that parametric yield ($/wafer after bin-sorting) is severely threatened by the growing process variability implicit in feature size and device architecture roadmaps. Advances in circuit and architecture design are considered to be possible remedies for the problem. The most important design trends are considered in the following section.

## 4. Design methods drivers

An important message in the ITRS 2001 roadmap [1] is that design cost is the greatest threat to continuation of the semiconductor industry's phenomenal growth. According to Intel, a 1981 leading edge chip required 100 designer months, contained 10,000 transistors, which makes 100 transistors per month. A 2002 leading edge chip required already 30,000 designer months and contains 150,000,000 making it 5000 transistors/month. However, the design costs have increased from $1M to $300M during the same period. Thus, the chip development capacity has increased 50 times at the same time as design costs have increased 300 times.

This dramatic increase in cost is mainly due to the fact that traditionally the IC capacity has grown 58%/year, while the designers productivity grows only 21 % annually. The phenomenon is shown in Figure 1 and is known as the design productivity gap [6]. It is the productivity gap that pushes the chip-making companies to exploit more and more engineering resources in order to reach the limits of what can be achieved in modern technology resulting in ever-increasing costs. Obviously, this gap could be contended and costs reduced only if more effective design approaches would be developed in the future to increase designer's productivity.

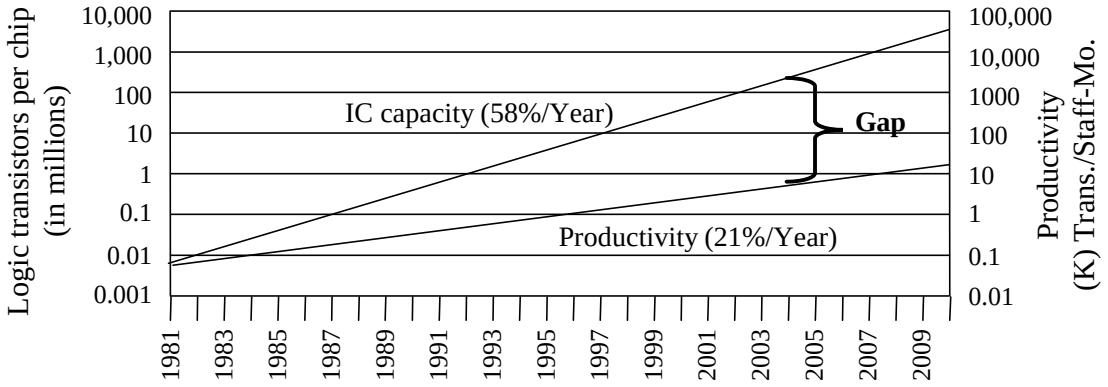


Figure 1. Design productivity gap.

The ITRS 2001 roadmap sees two types of complexity challenges for design: silicon complexity and system complexity. Silicon complexity refers to the impact of process scaling and the introduction of new materials or device/interconnect architectures. Silicon complexity places long-standing paradigms at risk: System-wide synchronization becomes infeasible due to power limits and the cost of robustness under manufacturing variability; the CMOS transistor becomes subject to ever-larger statistical variabilities in its behavior; and fabrication of chips with 100 percent working transistors and interconnects becomes prohibitively expensive [4]. System complexity refers to exponentially increasing transistor counts enabled by smaller feature sizes and spurred by consumer demand for increased functionality, lower cost, and shorter time to market.

Together, silicon and system complexity trends lead to superexponentially increasing design process complexity. To combat this complexity, eight methodology measures are called out for the future evolution of Design Technology (DT):

1) exploit reuse;
2) evolve DT rapidly;
3) avoid iterations;
4) replace verification by prevention;
5) improve predictability;
6) orthogonalize concerns (for example, by separating behavior from architecture, or computation from communication);
7) expand the scope of DT (up to package and board levels, down to mask and process, from digital hardware to software and AMS, and so on);
8) unify previously disparate subareas of DT.

The Roadmap sets out detailed challenges with respect to five traditional areas of DT: design process; system-level design; logic, circuit, and physical design; design verification; and test. However, beyond enumerating these detailed challenges, the 2001 Roadmap also identifies five *crosscutting challenges* that encompass all relationships between electronic design automation and the other industries that support the semiconductor industry whose solutions are distributed across all areas of design technology. The five challenges are productivity, power, manufacturing integration, interference, and error tolerance.

**Productivity**
To avoid exponentially increasing design costs, overall productivity of designed functions on chip—as well as reuse productivity (including migration) of design, verification, and test—must scale at more than two times per node. Verification has become a bottleneck that has reached crisis proportions, calling for reliable and predictable silicon implementation fabrics that support higher-level system design handoffs. Reducing DT time to market requires standards that promote stability, predictability, and interoperability [4].

**Power**
Nonideal scaling of planar CMOS devices, together with the Roadmap for interconnect materials and package technologies, presents a variety of power management and current delivery challenges. MPU power dissipation will exceed high-performance single-chip package power limits by 25 times at the end of the Roadmap [1], whereas low-power SoC drivers require flat average and standby power even as logic content and throughput continue to grow exponentially. DT must address the resulting power management gap in which increasing power densities worsen thermal impact on reliability and performance and decreasing supply voltages worsen switching currents and noise [4].

**Manufacturing integration**
Feasibility of future technology nodes will depend on sharing challenges within the industry as a whole. Die-package-board cooptimization and analysis may improve system implementation cost, performance verification, and overall design TAT as well as system-in-package DT. New DT for correctness under manufacturing variability—for example, variability-aware circuit design, design for regularity, timing-structure optimization, and static-performance verification—may relax

critical-dimension control requirements in the lithography, process integration, devices, and structures, front-end processing, and interconnect technology areas [4].

**Interference**
Noise and interference increasingly hamper resource-efficient communication and synchronization. Prevailing signal integrity methodologies in logical, circuit, and physical design are reaching their limits of practicality. Scaling and SoC integration of mixed-signal and RF components will require more flexible and powerful methodologies. A basic DT challenge is to improve characterization, modeling, and analysis and estimation of noise and interference at all levels of design [4].

**Error tolerance**
Error tolerance, correction, and self-repair could dramatically increase manufacturing yields but will require additional effort in verification and test. Technology scaling likely forces such a paradigm shift, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects. Below 100 nm, single-event upsets (soft errors) severely impact both memory and logic field-level product reliability. Atomic-scale effects demand new “soft” defect criteria, such as for noncatastrophic gate oxide breakdown [4].

In general, automatic insertion of robustness into the design will become a priority as systems become too large to functionally test at manufacturing exit. Potential measures include automatic introduction of redundant logic and on-chip reconfigurability for fault tolerance, development of adaptive and self-correcting or self-repairing circuits, and soft-ware-based fault tolerance [4].

## 5. Test technology drivers

In the beginning of the previous section we stated that the increasing design costs are the main threat to semiconductor industries future growth. However, it is the cost of test, which is taking ever-increasing percentage of the total design costs. Let us take a look at what are the main issues contributing to the rapid increase in test expenses.

Generating test vectors for digital circuits is a difficult task, which belongs to the class of NP-complete problems. Worst case test generation complexity grows exponentially with the number of circuit inputs and internal flipflops. Another issue that affects the test complexity is the decreasing accessibility of internal nodes of the chip. According to an empirical relation observed by IBM, which is known as Rent’ rule, the number of pins grows as a square root in respect to the number of transistors on chip. In other words, it is becoming increasingly difficult to access internal modules from the chip I/O in order to apply tests to them.

Another problem is the explosion of number of vectors to test the chip. Six years ago in 1997 a tester was capable of storing and delivering up to 64 million vectors, which takes just over 0.2 seconds to execute on a 300 MHz tester [5]. However, the roadmap shows that as the number of transistors per chip trends towards 180 million per square cm by 2012, the number of test vectors required will increase to 10 billion [5] (Figure 2). This amount of test data will be prohibitive, and the time to execute the test will reach around 10 seconds, even on a 1 GHz tester, pushing test times up by a factor of 50!

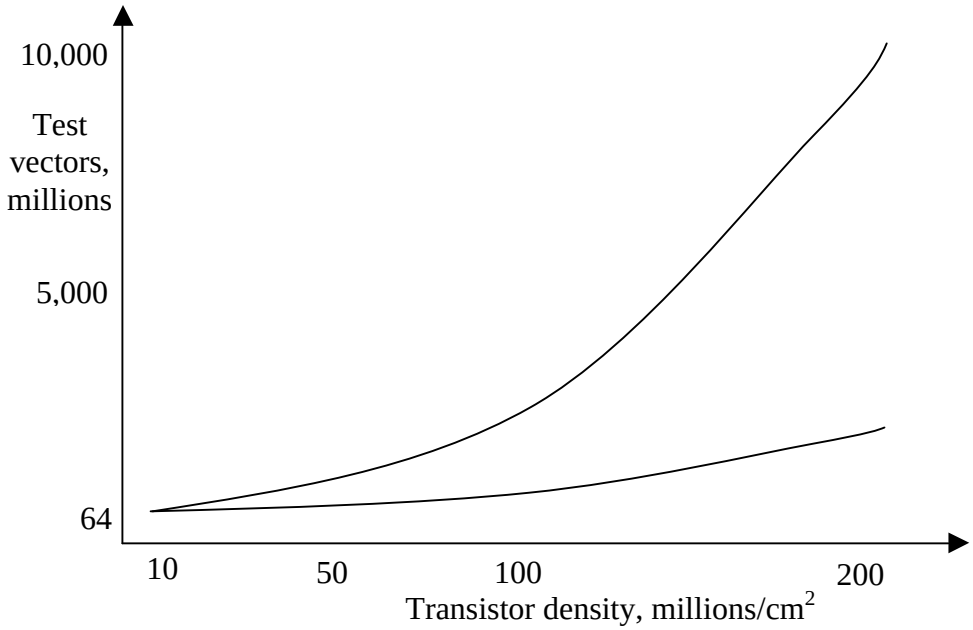


Figure 2. Number of test vectors as a function of transistor density

The solution to this problem is twofold. First, the Automated Test Equipment (ATE) industry should continue to develop test equipment that would test more complex chips at a faster speed. But this will probably not be enough. It is also important to incorporate more design-for-testability (DFT) structures to the chip silicon itself in order to share the load between the tester and the hardware under test (Figure 2). As we see later in this Section, this development has already started.

It is not only the test complexity that causes worries but also the trends in test equipment. While the Automated Test Equipment (ATE) cost per pin will stay nearly constant according to the roadmap [1] the increasing number of pins would push the total ATE costs from 2...5 mil $ to 25 mil $ by 2012. At the same time, manufacturing yield loss associated with the at-speed functional test methodology is related to the growing gap between ATE performance and the ever increasing device I/O speed as shown in the Overall Roadmap Technology Characteristics (ORTC) tables [1]. Increasing microprocessor and ASIC I/O speeds require increased accuracy for proper resolution of timing signals. While semiconductor off-chip speeds have improved at 30% per year, tester accuracy has improved at a rate of 12% per year. Typical headroom offered by testers five times faster than device speeds in the 1980s have disappeared. If the current trends continue, tester timing errors will approach the cycle time of the fastest devices. In 2001, yield losses due to tester inaccuracy are becoming a problem when using a traditional functional test methodology as shown in Table 2 [1].

Table 2. Predicted ATE accuracy versus required accuracy

| YEAR | **2003** | **2004** | **2005** | **2006** | **2007** |
|---|---|---|---|---|---|
| Chip-to-Board Bus Frequency High Performance, MHz | 2057 | 2262 | 2488 | 2737 | 3011 |
| Device period, ps | 486 | 442 | 402 | 365 | 332 |
| Overall ATE accuracy (OTA), ps | 155 | 136 | 120 | 106 | 93 |
| Overall device accuracy requirements (5% target), ps | 24 | 22 | 20 | 18 | 17 |

At the time the latest roadmaps were being developed expensive multi-million $ ATE equipment was all that was available. However, if as the roadmaps predict, the ATE becomes ever-more expensive at the same time as the its at-speed test capabilities decrease, adding Built-In Self-Test (BIST) structures to the chip will become motivated. This would also give a boost to adoption of low-cost Design-for-Testability (DFT) testers, which have, in fact, already started to appear. Very recently such market has emerged with a whole range of new startup companies like Teseda, Inovys and NPTest offering their products. [8]. These are PC-based units, whose prices can be as low as 60 thousand $. One of the main motivating drivers for the appearance of the new industry of low cost-testers is the above-mentioned rapidly increasing price of traditional ATE. The other driver is the fact that there is more DFT (BIST, test data compression, internal scan, etc.) implemented in modern chips to support e.g. at-speed testing than it has been available in the past. This concept of moving test hardware from the tester to the chip is refered to as *test resource partitioning*. It is clear that the above breakthrough strongly influences the evolution of test technology and therefore it should be taken into account in the development of future technology roadmaps.

Future issues in testing include need for adoption of low power test methods and improvements to IDDQ current testing. With high power dissipation of modern devices it is increasingly probable that the test patterns (e.g. pseudorandom test patterns of BIST or scan patterns) will simply burn the chip. Thus, low power ATPG and/or functional test methods are required in the future.

Another trend is that normal background leakages (both the amplitude and variability) are increasing to the point where IDDQ testing as it has historically been practiced for identifying defect-driven reliability failures will face difficulty in the future. IDDQ testing must change to continue to enable defect detection. Alternative solutions must be developed to provide the same benefits in the face of the rising background leakage currents of future technologies. IDDQ provides a rich source of information about a manufactured chip and in many cases today plays a vital role in both defect detection and characterization [1].

## 6. Implications to Estonian research and industry

The most important implication to Estonian SME is the rapidly increasing development cost of the leading edge design, which has reached already 300 million dollars by now. This is far beyond the reach of the entire national sector. Moreover, in that context even the largest enterprises in the Nordic area, Nokia and Ericsson should be considered as SMEs...

Another important message is that new, more powerful design, verification and test methods are urgently needed to help keeping the costs down. In addition, as the roadmap shows it is also important to have a more integrated view to different design tasks, rather than considering them independently as it was done in the traditional waterfall approach.

As a conclusion, TTU research in the fields of automated circuit synthesis, test and design-for-testability is potentially extremely valuable for local digital electronics companies to increase their competitiveness. In fact a lot of cooperation in the form of applied research, common master theses and practical placements has taken place during recent years between the Department of Computer Engineering and Estonian chip-maker company Artec Design Ltd. In 2001, TTU and Artec Design signed a contract to regulate the cooperative activities. In addition, in 2003 TTU (with international companies like JTAG, Xilinx, National Semiconductor, National Instruments) organized four educational workshops and courses for the local electronics SMEs.

## 7. Conclusions

Current report considered the main developments in semiconductor industry according to the leading roadmaps. System drivers, the main challenges in the design area and the trends in test methods, tools and the Automatic Test Equipment (ATE) were presented. The impact of the developments foreseen by The International Technology Roadmap for Semiconductors (ITRS) to the Estonian research community and industry in the microelectronics field was discussed.

While the ITRS roadmaps have become more sophisticated year-by-year there still seems to be some shortcomings. For example, in the design section it is pointed out that the productivity is the main issue as the old-fashioned waterfall approach to design is not sufficient anymore and an ‘integrated’ approach with design reuse should be implemented instead. However, no suggestions to wider acceptance of HW/SW codesign or behavioral synthesis approaches are made in the roadmap. Also, in the “Test and Test Equipment” section the progress relies merely on Built-In Self-Test (BIST) and Design-for-Testability (DFT). Thus, no breakthrough in test generation methods is predicted to happen in the following 15 years range.

In addition some other details have been left out of consideration. For example, in the “Environment/health” section the contamination caused by chip production itself is taken into account while the ever-increasing power-hungryness of the devices predicted by the roadmap puts additional strain to the environment, which has been neglected in the document.

Despite of the shortcomings and the fact that it is really not possible to predict the future accurately the roadmaps have been useful in planning future research and even promoted establishing new industries as in the case of low-cost testers. Hopefully, current research topics like HW/SW codesign, behavioral synthesis, high-level test generation etc. will finally break in to the roadmaps and later to the industry mainstream in order to boost designers productivity. Because it is the low productivity that sky-rockets the costs of chip development and thus threatens to slow down the growth of the semiconductor industry.

## References


[1] *The International Technology Roadmap for Semiconductors, 2001 edition*. International Sematech, Austin, Texas, 2001.

[2] *The International Technology Roadmap for Semiconductors, 2002 update*. URL: http: //public.itrs.net/

[3] *The National Technology Roadmap for Semiconductors*. Semiconductor Industry Association, 1997.

[4] A. Allan, D. Edenfeld, W.H. Joyner, A.B. Kahng, M. Rodgers, Y. Zorian. 2001 Technology Roadmap for Semiconductors. *IEEE Computer*, January 2002, pp. 42-53

[5] R. Leckie. The Test Technology Roadmap. *Semiconductor Fabtech – 8th edition*, pp. 309-314.

[6] K.Keutzer, R.Newton. SEMATECH. ( http://www.sematech.org/public/home.htm)

[7] M.L. Bushnell, V.D. Agrawal. *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*. Kluwer Academic Publishers, 2000, 690 p.

[8] R.G. Bennetts, Low-cost PC-based chip DFT testers, *Chip test course*, Bennetts Associates, September, 2003.