EVikings II

Establishment of the Virtual Centre of Excellence for IST RTD in Estonia

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1. INTRODUCTION

Electronic systems are becoming ubiquitous and their reliability issues are present in all types of consumer applications. In order to guarantee a high level of reliability, adequate testing of electronic products is required. However, testing contemporary electronic systems is an extremely hard task. Furthermore, the ever-increasing complexity of these systems causes the need for new, more efficient test methods.

The general aim of the work package was to strengthen and support research and development activities in line with the MEDEA roadmap in design and test of digital systems, and implementation of new research results as innovative new CAD tools in the local industry. The goal was also to strengthen international research contacts via mutual co-operation with European research institutions.

The research in this workpackage was carried out in a broad field of digital design and test. The following topics were covered: design for testability, fault modeling and fault analysis, reconfigurable hardware based accelerators for fault simulation, test generation, design of self-testing systems. A lot of useful results have been achieved and published in a recognized journals and proceedings. Continuous experimental work has been carried that was needed for proving the efficiency of new algorithms and methods. As a result, a lot of prototype tools were created and combined in a multi-functional CAD environment that has been used both for research and teaching purposes. This environment was and is being used for several projects with Estonian industry. New testing methodologies were developed and experimented in cooperation with company Artec Design. Novel BIST ideas are being developed and used for industrial purposes in a Technology Development Centre ELIKO: a new national centre uniting Estonian microelectronics SMEs and Tallinn University of Technology to carry out applied and basic research projects. New Boundary Scan and interconnect testing methods developed in the project will be now the content of the new industrial projects to be contracted with Testonica Lab in Estonia and with Ericsson AB and SAAB in Sweden.

The new quality and originality of the environment developed in the project is in the property of multi-functionality of the system (important for research and training), low-cost and ease of use. The multi-functionality means that different abstraction level models can be easily synthesized and resynthesized (to analize the influence of the complexity of the model to the efficiency of methods), the methods are implemented by different algorithms (to analize the efficiency of different approaches), the fault models can be easily changed and updated (to analyze the adequacy and accuracy of testing). The multi-functionality allows to set up and modify easily different experimental schemes and scenarios for investigating new ideas and methods. It gives an excellent opportunity for students to understand the ideas, advantages and drawbacks of different methods at changeable conditions. In traditional commercial design tools these purely research oriented possibilities are missing. On the other hand, in many cases the commercial tools can be replaced by new tools developed in WP4 in small design companies also for commercial design purposes, because of their low-cost and ease of

use compared to the very expensive commercial systems.

Based on this environment intensive international cooperation has been carried out which has resulted in a lot of joint research results and publications with international partners from more than 10 countries. 6 international conferences and workshops were organized in WP3 during the project years instead of only three that were initially planned. We had all together 14 student placements at international partner institutions, and 3 placements in the industry. This helped to strengthen the cooperation with industry and with international academic world. As the result we published during the last 3 years all together 50 joint papers with foreign co-authors where the initiative belonged mostly to our researchers, and where the main experimental research was carried out in the environment created as the result of the project.

Thanks to the project, an intensive cooperation has been started with several academic and research institutions in Estonia, like Tartu University (2 joint papers, a placement of a PhD student at TU Tallinn, joint seminars in Tartu and Tallinn), Institute of Cybernetics (joint tasks in the projects of ELIKO) etc.

The cooperation between other WPs of the project was targeted to organization of joint courses and seminars. For example, at Computer Theory Days organized by Institute of Cybernetics (WP2), October 3-5, 2003, DCE lecturers (involved in WP4) held a full session on digital microelectronics design: Prof. P. Ellervee "High-level synthesis and hardware compilation", Prof. K. Tammemae "Co-design: from practice to theory. There are joint projects of people involved in WP2 and WP3 that are coordinated by the development centre ELIKO which itself can be regarded as a “product of the current project”.

The project helped considerably to strengthen the level of teaching design and test topics in the curricula at TTU. A full cycle of digital design and test courses were developed in WP4. The created E-learning environment for Web-based study of design and test allowed to make teaching more attractive and efficient. It also allowed to engage better MSc and PhD students in the research activities of the group which is very important for maintaining the momentum of future research in the current field of designing and testing of SoC and NoC.

2. MAIN RESEARCH RESULTS

The increasing complexity of electronic systems has made testing one of the most complicated and time-consuming problems in system design and production. The rapid developments in the areas of deep-submicron electron technology and design automation tools are enabling engineers to design larger and more complex electronic systems. According to the Moore's law, the computer power doubles roughly every 18 months. This means that since 1950 the computer power has increased by a factor of about 10 billions. This increase is larger than the transition from chemical explosives to the hydrogen bomb.

The more complex are electronic systems getting the more probable will be the failures, and the more important will be the problems of testing. Nanometer technologies introduce new formidable challenges making test quality a very fast moving target. The importance of test and design for testability is growing because the expenses of verification and test are becoming the major components of the design and manufacturing costs of new products.

The main problems in the test field are related to the continuously growing complexity of systems which make testing and fault diagnosis extremely difficult. New hierarchical approaches are needed to cope with the growing complexity and the testing quality needs.

Several novel conceptions were introduced, developed and investigated in the project:

- uniform approach to hierarchical diagnostic modeling of digital systems based on using decision diagrams;
- new conception of mapping faults from one hierarchical level to another based on a novel functional fault model;
- a conception of hybrid self-testing architectures where slow but exact deterministic testing methods are optimally combined with fast and not exact on-line testing methods;
- combining of reconfigurable hardware and software to increase the efficiency of traditionally by software solved algorithmic solutions in the design and test field.

Based on these novel conceptions, the main research activities that took place in WP4 can be split into the following different topics:

- Decision diagrams for diagnostic modeling of digital systems
- Fault modeling and a new uniform fault model
- A new defect oriented deterministic test generator
- Hierarchical automated test generation with decision diagrams
- Hybrid built-in self-test in Systems-on-Chip
- Network-on Chip interconnect testing
- Fault simulation accelerator based on reconfigurable hardware
- Design for testability

- Creating a multifunctional research environment
- E-learning environment for Web-based study of testing

A short overview of the content of research and the achieved results in the listed topic areas will follow. The references are to the publications produced in the frame of the project during the years 2003-2005.

2.1. Decision Diagrams for Diagnostic Modeling of Digital Systems

Hierarchical approach was the main methodology we used in solving the test problems for complex digital systems. As the mathematical basis we used a new original diagnostic model for digital systems – Decision Diagrams (DD), developed by the group. The well known Binary Decision Diagrams (BDD) can be considered as a particular case of this model. DD-s allowed us to investigate and solve the problems of test synthesis and analysis uniformly at different abstraction levels of digital systems.

For logic level diagnostic modeling we developed a special class of BDDs – structurally synthesized BDDs (SSBDD) to represent the topology of gate-level circuits in terms of signal paths. Unlike "traditional" BDDs, SSBDDs directly support test generation for gate-level structural faults without representing these faults explicitly. The advantage of the SSBDD based approach is that the library of components is not needed for structural path activization. This is the reason why SSBDD based test generation procedures do not depend on whether the circuit is represented on the gate level or on the macro-level whereas the macro means an arbitrary single-output subcircuit of the whole circuit. This independence makes SSBDDs extremely efficient for hierarchical logic level test generation. Several new interesting features were discovered in the SSBDD model which allowed to increase the simulation speed on SSBDDS [3,4,61,67].

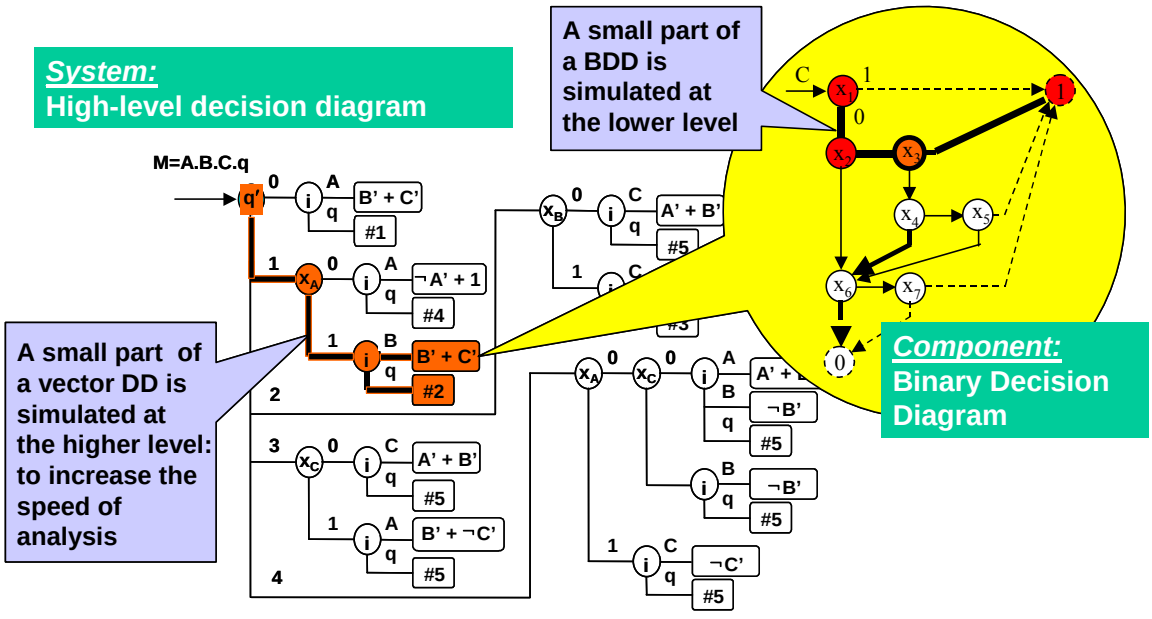

Figure 1. Hierarchical modeling with DDs

The drawback of traditional multi-level and hierarchical approaches to digital test lies in the need of different dedicated languages and models for different levels. Using DDs we were able to develop uniform methods for hierarchical diagnostic modeling of digital systems.

It came out that the methods developed for Binary DDs were suitable for generalization for using them also for higher level DDs [9,44,84]. Several methods were developed to compress the high-level DD-model to further increase the simulation speed. Examples are complex DDs where a group of simple high-level DDs representing several high-level components are joined into a single vector DD. In vector DDs the parts of different high-level components can be simulated in parallel.

In Figure 1 the idea of hierarchical diagnostic modeling is illustrated. A small part of a vector DD is simulated. When an error is detected, and located to the high level component (adder) *B+C*, then the adder can be represented more exactly at the lower logic level for exact fault location in the logic circuits with accuracy of signal lines or gate-level components.

New results:

1. Recent research showed that generalization of BDDs for higher levels provides a uniform fault model for both gate and RT level or even behavioral level fault modeling, fault simulation and test generation [54, 80].
2. Based on SSBDDs and high level DDs new efficient hierarchical methods for logic level fault simulation [2,12,93] and test generation [18], hierarchical fault simulation [65,86] and test generation [21,55,69,102] were developed.

2.2. Fault Modeling and a New Uniform Fault Model

As the complexity of digital systems continues to increase, the traditional low level diagnostic analysis methods have become obsolete. Other approaches based mainly on higher level functional and behavioral methods are gaining more popularity.

However, the trend towards higher level modeling moves us even more away from the real life of defects and, hence, from accuracy of testing. To handle adequately defects in deep-submicron technologies, new fault models and defect-oriented test methods should be used. On the other hand, the defect-orientation is increasing even more the complexity.

To get out from the deadlock, the two opposite trends – high-level modeling and defect-orientation – should be combined into hierarchical approaches. The advantage of hierarchical approaches compared to high-level functional modeling lies in the possibility of constructing test plans on higher levels, and modeling faults on more detailed lower levels.

Consider a Boolean function $y = f(x_1, x_2, \ldots, x_n)$ of a component (library cell) C in a circuit. Introduce a Boolean variable d for representing a given physical defect in the component, which converts f into another faulty function $y = f^d(x_1, x_2, \ldots, x_n)$. Introduce for C a generic function

$$y^* = f^*(x_1, x_2, \ldots, x_n d) = \bar{d} f \vee d f^d \qquad (1)$$

which describes the behavior of the component simultaneously for both fault-free and faulty cases. The solutions of the equation

$$W^d = \frac{\partial y^*}{\partial d} = 1 \qquad (2)$$

describe the conditions which activate the defect d to a line y. The conditions W^d allow to map physical defects d to logic level. The constraint $W^d = 1$ defines how a lower level fault d should be activated at a higher level to a given node y.

A pair (W^d, y) was defined as a uniform abstract functional fault model for a physical defect or for a group of physical defects, free from any details of the real defects it is representing

[16,18 (best paper award)].

On the other hand, this model can be regarded as an interface for mapping faults from one system level to another, helping to carry out hierarchical test generation.

In the described approach we have to characterize all possible defects in all library cells, and represent the results as defect tables. The defect characterization may be computationally expensive, but it is performed only once for every library cell.

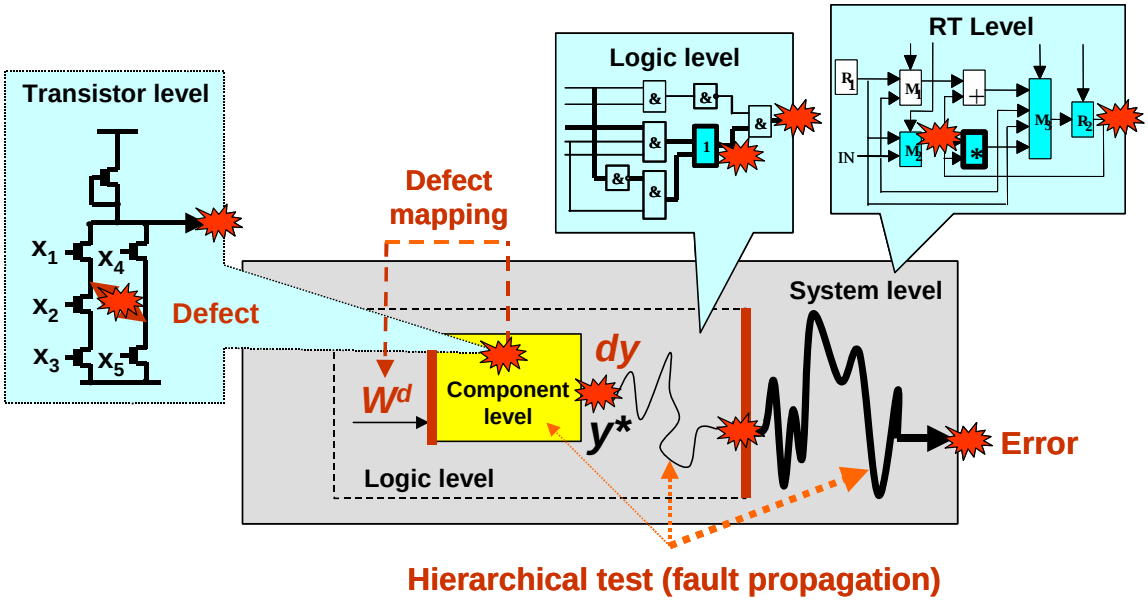

Figure 2. Hierarchical test generation and fault simulation

In Figure 2, an example of a hierarchical fault activation and propagation for test generation purposes is illustrated. A physical defect in a component (library cell) at a low transistor or layout level is mapped as a logic condition $W^d = 1$ to the logic level and the result of mapping as a functional fault (W^d, y) is stored in the cell library. The erroneous signal dy on a line y is propagated on the logic level to an output of the corresponding logic level module, and thereafter on the higher level (register transfer or instruction set level) from this point to an observable point (to primary output or to memory for storing) for observing as an erroneous signal.

New results:

1. The new functional fault model allows to handle arbitrary physical defects by purely logic methods and algorithms [80,92].
2. The model creates a simple conception and basis for hierarchical test generation and fault simulation [90].

2.3. A New Defect-Oriented Deterministic Test Pattern Generator

A method was developed for deterministic test pattern generation using a uniform functional fault model for combinational circuits. The fault model allows to represent arbitrary physical defects in components and defects in the communication network of components by the same technique. Physical defects in components are modeled as parameters in generic Boolean differential equations. Solutions of these equations give the conditions $W^d = 1$ for activating defects locally. The possibility of detecting the bridging faults that via feedback will

transform a combinational circuit into a sequential one is also created. A method is proposed which allows to find the types of faults that may occur in a real circuit and to determine their probabilities.

A defect-oriented deterministic test generation tool was developed (DOT), and the experimental data obtained by the tool for benchmark circuits are presented in Table 1. It was shown that 100% stuck-at fault tests covered only about 75-82% physical defects (column 5 in Table 1). The main feature of the new tool is its ability to reach 100% defect testing efficiency (percentage of covering the nonredundant defects) for the given set of defects by proving the redundancy of not detected defects. The tool allows to prove the redundancy of physical defects in relation to the logic behaviour of a circuit. Such a function of the tool to prove the redundancy of physical defects to our knowledge in unique in the world.

Column 6 in the Table 1 shows the defect testing efficiency after proving the redundancy of defects inside the library cells, and column 7 shows the defect testing efficiency after proving the redundancy for the whole set of defects. The column 8 shows the defect testing efficiency reached by the test generation tool DOT.

Table 1. Experimental data of defect-oriented test generation

Circuit	Number of defects			Defect coverage			
	All defects	Redundant defects		100% stuck-at fault ATPG			DOT
		Gates	System				
1	2	3	4	5	6	7	8
c432	1519	226	0	78,6	99,05	99,05	100,00
c880	3380	499	5	**75,0**	99,50	99,66	100,00
c2670	6090	703	61	79,1	98,29	**98,29**	100,00
c3540	7660	985	74	80,1	98,52	99,76	99,97
c5315	14794	1546	260	82,4	97,73	99,93	100,00
c6288	24433	4005	41	77,0	99,81	100,00	100,00

This work on defect-oriented testing has been carried out in a cooperation between TU Darmstadt (Germany), University of Technology in Warsaw (Poland) and TU Tallinn.

The main results of this research are published in the papers [27,37,38].

New results:

1. The first time a tool was created for proving redundancy of physical defects. This feature of the tool allows to evaluate the quality of test generation more adequately than the existing tools can do [27,37,38].
2. The new tool allows to reach 100% defect coverage, that other existing tools cannot do because they miss the accurate measure [17,73,79].
3. The model creates a simple conception and basis for hierarchical test generation and fault simulation [90].

2.4. Automated Test Pattern Generation with Hierarchical DDs

The following research was carried out in the field of hierarchical test pattern generation. New fault models for multiplexers in hierarchical designs were developed. The new models covered 100 % of stuck-at faults in multiplexers embedded to datapaths. Additional important

result was development of fault models to target conditional operators in digital systems [54]. Both fault models were implemented and tested on a hierarchical test pattern generation tool DECIDER[1] created at Tallinn University of Technology. The experiments showed significant improvement in comparison to state-of-the-art test generation approaches.

In the following, we will explain the fault models implemented in current approach, where a combination of three fault models is used. These include a hierarchical fault model for Functional Units (FU), a functional model for multiplexers [55] and a combined hierarchical-functional model for conditional operations [254. Circuit areas targeted by each of the above models are marked in Fig. 1 by grey circles.

2.4.1. New functional fault models for multiplexers

Makar and McCluskey[2] presented the groundwork for deriving minimal tests for AND/OR, OR/AND and nMOS implementations of multiplexers. The functional fault model developed in the framework of e-Vikings II project is similar but it extends it with the ability to cover multiple stuck-at faults at the address select inputs of the MUX under test. This, in turn, provides for potentially better coverage of faults in the output logic of the control part FSM.

The new functional model is based on distinguishing values at the data inputs of the MUX. For multiplexers having more than two data inputs we have chosen to implement pair-wise distinguishing of data inputs as opposed to distinguishing all the inputs simultaneously. The main motivation for that is that high-level path justification from all inputs may be difficult to achieve. Moreover, it can lead to inconsistencies and therefore to loss of solutions.

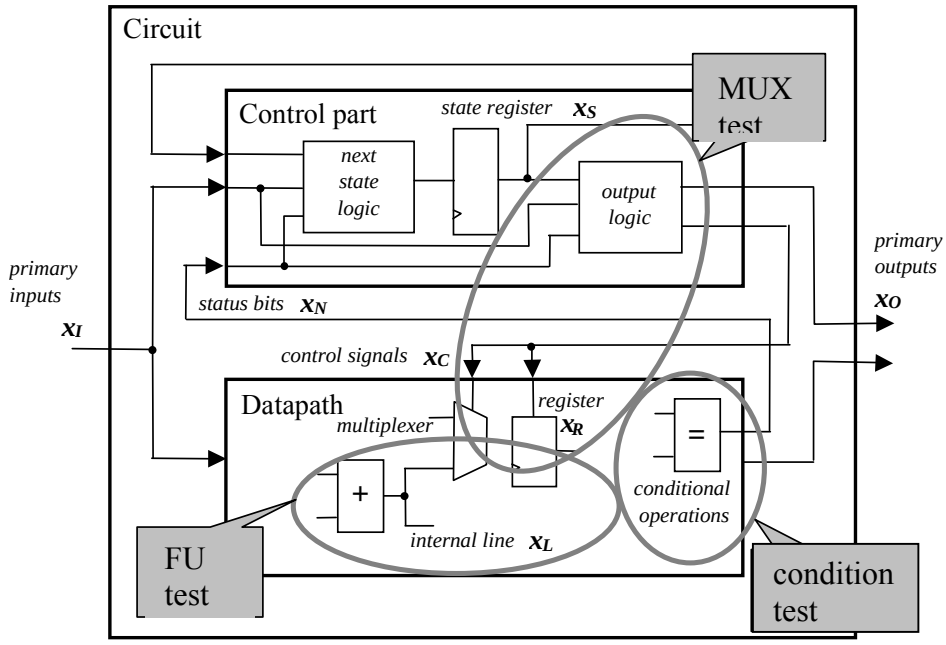

Figure 3. Coverage of new hierarchical fault models

[1] J.Raik, R.Ubar. Fast Test Pattern Generation for Sequential Circuits Using Decision Diagram Representations. *Journal of Electronic Testing: Theory and Applications*, Kluwer Academic Publishers. Vol. 16, No. 3, pp. 213-226, June, 2000.

[2] Makar, S.R., and E.J. McCluskey, "On The Testing Of Multiplexers," Proc. 1988 Int. Test Conf., Washington, DC, pp. 669-679, September 12-14, 1988.

Note, that treating MUXs by a hierarchical fault model similar to the one used for FUs would not have allowed targeting faults in the control part. Furthermore, a slow, three-valued fault simulator would have been needed for evaluating the fault coverage achieved in the multiplexers at the low level. In current work, only AND/OR multiplexers are considered but functional models for other multiplexer types can be derived in a similar way. (e.g. the fault model for OR/AND multiplexers is dual to AND/OR[3]).

2.4.2. Fault model for targeting conditional FUs

The main novel contribution of the project is the new fault model for targeting conditional operations in RTL designs [54]. By conditional operations we mean FUs, whose outputs are used as status bits (or flags) entering the FSM. Here, usually comparison functions are implemented but also outputs of arithmetic and logic functions can be connected to status bits. The main difficulty in testing such modules lies in the fact that no propagation path to primary outputs through the datapath exists for them.

A combined functional hierarchical fault model is used for testing the conditional operations. A functional approach is selected to activate the fault effect at the output of the module under test. Additionally, a hierarchical model [13] is implemented to test the module at the low level. The experimental results showing the improvement provided by the new fault models are presented below.

2.4.3. Experimental results

In Table 2, comparison of test generation results of four ATPG tools are presented on six hierarchical benchmarks. The other tools considered in the comparative experiments include HITEC[4], which is a logic-level deterministic ATPG, GATEST[5] as a genetic-algorithm based tool and a hierarchical ATPG DECIDER[6]. The column 'current approach' shows the results obtained by the functional-hierarchical method developed in e-Vikings II project.

Table 2. Comparison of sequential circuit test generation tools

circuit	faults	HITEC[4]		GATEST[5]		DECIDER[6]		current approach	
		F.C., %	time, s	F.C., %	time, s	F.C., %	time, s	F.C., %	time, s
gcd	454	81.1	169.5	**91.0**	75	89.9	13.5	89.9	129.8
sosq	1938	77.3	728.4	79.9	739	80.0	79.3	**80.1**	129.6
mult8x8	2036	65.9	1243	69.2	821.6	74.1	50.2	**74.7**	93.7
ellipf	5388	87.9	2090	94.7	6229	**95.04**	1197.8	**95.04**	1258.9
risc	6434	52.8	49,020	96.0	2459	95.8	85	**96.5**	150.5
diffeq	10,008	96.2	13,320	96.40	3000	96.51	295.5	**97.09**	453.7
average F.C.:		76.9		87.9		88.6		**88.9**	

[3] Makar, S.R., and E.J. McCluskey, "On The Testing Of Multiplexers," Proc. 1988 Int. Test Conf., Washington, DC, pp. 669-679, September 12-14, 1988.

[4] T. M. Niermann, J. H. Patel, "HITEC: A test generation package for sequential circuits", Proc. European Conf. Design Automation (EDAC), pp.214-218, 1991.

[5] E. M. Rudnick, J. H. Patel, G. S. Greenstein, T. M. Niermann, "Sequential Circuit Test Generation in a Genetic Algorithm framework," Proc. DAC., pp. 698-704, 1994.

[6] J.Raik, R.Ubar. Fast Test Pattern Generation for Sequential Circuits Using Decision Diagram Representations. *Journal of Electronic Testing: Theory and Applications*, Kluwer Academic Publishers. Vol. 16, No. 3, pp. 213-226, June, 2000.

The experiments were run on a 366 MHz SUN UltraSPARC 60 server with 512 MB RAM under SOLARIS 2.8 operating system. Actual stuck-at fault coverages of the test patterns generated by all the tools were measured by the same fault simulation software. The test generation times for the proposed method include both, test generation time and evaluation of the gate-level stuck-at fault coverage by the fault simulator.

In Table 2, fault coverages and run times in seconds for each example circuit are presented. The average fault coverage achieved by each tool is reported in the last row. Experiments show that the proposed method reaches the best fault coverage for five out of six examples. At the same time the run times of the hierarchical-functional approach are generally shorter than that of the simulation-based method GATEST and the deterministic ATPG HITEC. While the hierarchical approach published in [3] is slightly faster, its fault coverage in the case of three examples remains lower in respect to the proposed approach. Moreover, increasing the time-out for method [3] did not improve the results.

New results:

1. New fault models for multiplexers in hierarchical designs were developed [54,55].
2. The ATPG tool developed for using the new fault models reaches the best fault coverage compared to the known university tools whereas commercial hierarchical ATPG tools are missing [13,69,54,55].

2.5. Hybrid Built-In Self-Test in Systems-on-Chip

Due to the requirements for the Automatic Test Equipment (ATE) speed and memory, the ATE-based test solution may not always be affordable in terms of cost and accuracy. Therefore, in order to apply at-speed tests and to keep the test costs under control, on-chip, built-in self-test (BIST) solutions are becoming a mainstream technology for testing complex electronic systems.

Different test scenarios are possible, while using BIST. Sometimes the embedded cores may be tested using only internally generated pseudorandom test patterns. Due to several reasons, like very long test sequences, and random pattern resistant faults, this approach may not always be efficient.

One solution to this problem is to complement pseudorandom test patterns with deterministic test patterns, applied from the on-chip memory or, in special situations, from the ATE. This approach is usually referred to as hybrid BIST. One of the important parameters influencing the efficiency of a hybrid BIST approach is the ratio of pseudorandom and deterministic test patterns in the final test set. As the amount of resources on the chip is limited, the final test set has to be designed in such a way that the deterministic patterns fit into the on-chip memory. At the same time the testing time must be minimized in order to reduce testing cost and time-to-market.

Close cooperation in between Tallinn University of Technology and Linköping University, Sweden has given several original results in the area of hybrid BIST. The results have been reported in many high-quality conferences, like DFT, ATS, ETS, in 2 book chapters (published by Springer) and summarized in a monograph “Hybrid Built-In Self-Test and Test Generation Techniques for Digital Systems” (238 pages).

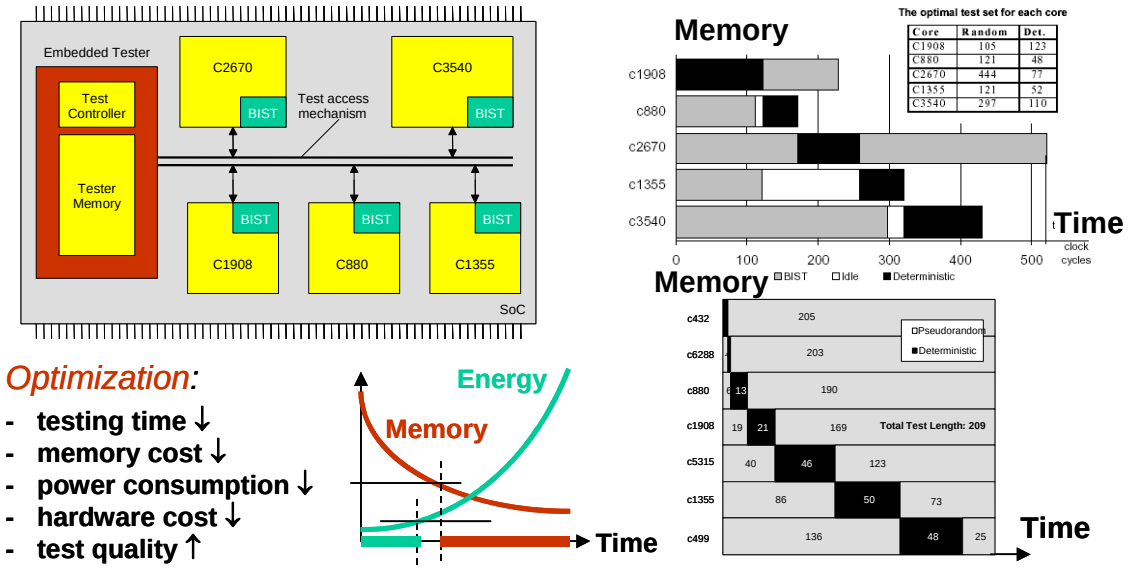

Figure 4. Optimization of hybrid built-in self-test

The main results have been so far a set of novel test cost minimization algorithms (minimization of testing time, memory cost, energy or power consumption, hardware cost) at the demanded test quality and at different design constraints.

We have developed algorithms and methods for test cost calculation together with global hybrid BIST optimization for single-core designs, and under memory constraints for multi-core systems. The methodology is based on a novel idea of cost estimation which allowed developing a fast iterative algorithm to minimize the total length of the hybrid BIST under given memory constraints. In addition we have developed a method for power-constrained system-on-chip test scheduling in an abort-on-first-fail environment where the test is terminated as soon as a fault is detected and proposed a technique to find the best ratio of pseudorandom and deterministic test sequences so that the total energy is minimized and the memory requirements for the deterministic test set are met without sacrificing test quality.

In Figure 4 a multi-core System-on-Chip is presented where all the cores have individual pseudorandom test generators which can work in parallel. A central test controller is coordinating the whole test process and his task is also to apply deterministic test sequences stored in the central memory to all the cores sequentially. The grey parts of test processes on the diagrams on the right show pseudorandom sequences, and the black parts show deterministic sequences. The upper diagram shows a randomly composed test process, the lower diagram shows the optimized one.

We have developed a novel hybrid functional BIST (HyBIST) scheme to combine the functional routines (working routines) carried out in digital systems with additional stored deterministic test patterns for testing microprogrammed data-paths in digital systems [58.68]. In the first test phase (see Figure 5) only the functional resources of a system (register file and data part) are used for testing purposes. A functional microprogram is carried out to control the data-path based on some deterministic input data. A response compressor like signature analyzer is connected to the data path to monitor the process. To quarantee a high test coverage for BIST, the second phase of the test is used which consists of applying additional deterministic test patterns pregenerated by an ATPG to test the random-pattern-resistant faults. Another option could be to improve the controllability and observability of the data part regarding the particular functional test.

A method is proposed to find the tradeoff between the functional test and deterministic test parts. Experimental research demonstrated the feasibility of the approach, and showed the advantage of combining functional and deterministic test patterns compared to the pure deterministic test or pure functional test.

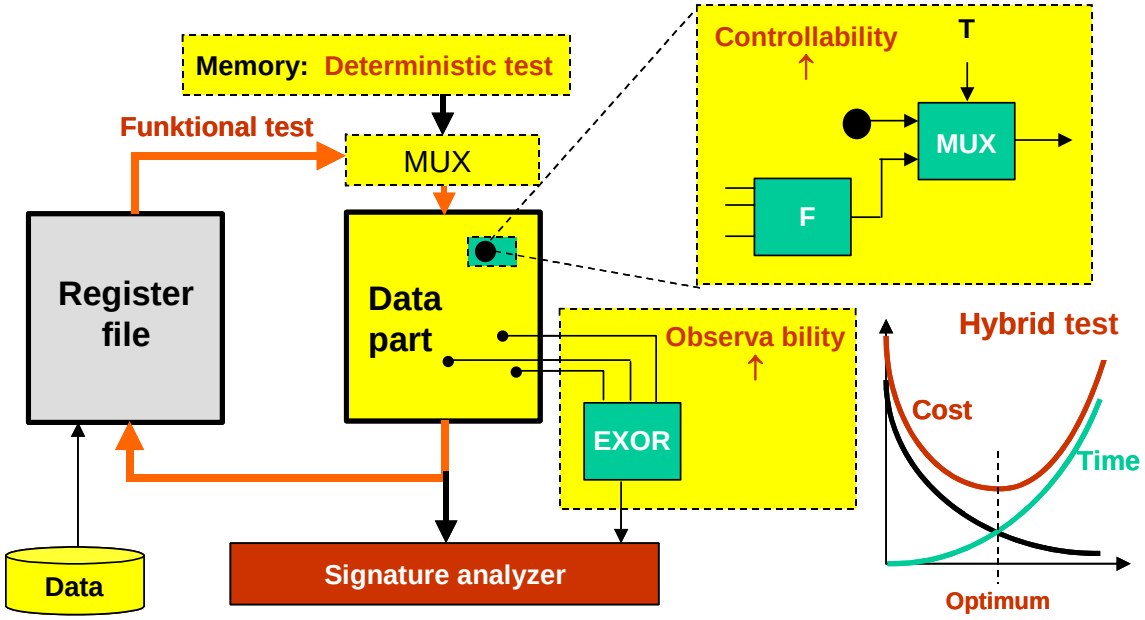

Figure 5. Hybrid functional built-in self-test

New results:

1. A novel method for fast cost estimation for variations of test processes with complex structure [35,50,77].
2. Based of the fast cost estimation method, very efficient iterative methods were developed for optimizing hybrid sequential and parallel test processes at different constraints [5,26,52,60,95-97].
3. A conception and implementation of functional BIST was proposed that allows to reduce considerably the hardware cost compared to the traditional BIST methods [58,68].

2.6. Network-on-Chip Interconnect Testing

The advances in semiconductor technology will soon allow us to build systems on chips (SoCs) with billions of transistors running at gigahertz frequencies. The bus-based interconnect paradigm widely spread in the board-level systems, lose its prevalence in the SoC world due to extremely high communication complexities of the modern multi-core systems. For the sake of robustness, flexibility, and scalability the bus-based interconnect architecture is being substituted by a packet-switching communication paradigm borrowed from data and computer networking. This new paradigm called Network on Chip (NoC) will be likely to use Globally Asynchronous Locally Synchronous (GALS) approach in order to avoid clock distribution problems in future chips. In GALS designs, a system is partitioned into multiple domains, each having a different clock.

Testing of NoC involves testing of the infrastructure's functional elements (routers/switches)

and conductive interconnect lines. This research concentrates on interconnect testing, which becomes an extremely important challenge due to the gigahertz operating frequencies and small gaps in the wires of high density chips. In such conditions, the crosstalk among interconnections is becoming a critical issue. Because of small dimensions, variations in the fabrication process are also affecting signal integrity and delays. The results of the current research can be classified by two directions: 1) solving the test application and fault detection problem in GALS structures and 2) design of a reconfigurable embedded test generation solution that supports a tradeoff between test speed and test quality and is designed for multi-layer on-chip interconnect structures. Both methods primarily target delay faults and harmful interference due to crosstalk.

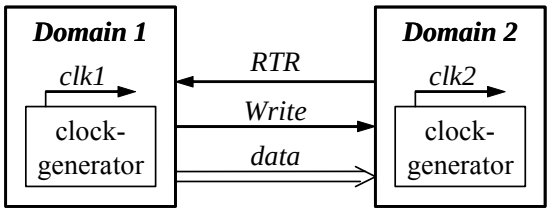

Fig.6. Connections in a handshaking protocol.

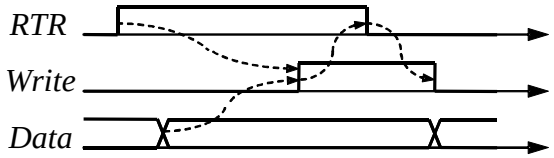

Fig.7. Data transfer through handshaking

In NoC based architectures, unidirectional physical channels are preferred between two resources or routers for communication, which, accordingly to the GALS paradigm, is asynchronous and uses handshaking signals (Fig.6 and 7). In such paradigm, signals *Write*, *RTR* (Ready-To-Receive) and *Data* are synchronized to the clocks in respective domains. The receiver asserts *RTR*=1 when it is able to receive new data. The transmitter sends the *Write* signal, which is followed by data transmission.

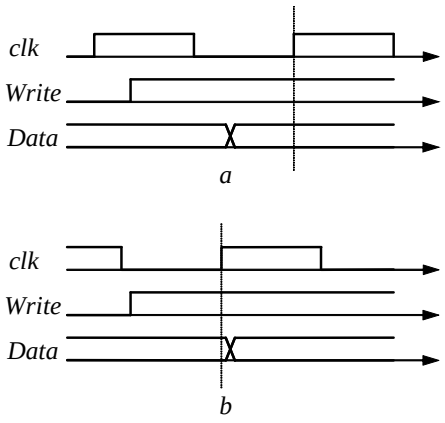

Fig.8. Signals at the receiver when data is delayed

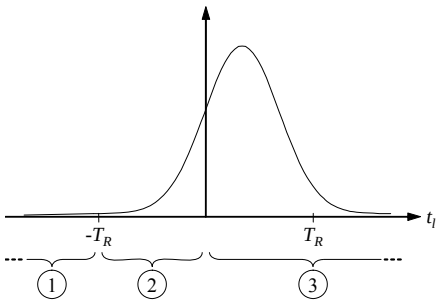

Fig. 9. Characteristics for t_l

Because there is no synchronisation between the clocks in the transmitter and receiver, the new data as well as *Write* can arrive in any part of the clock cycle of the receiver. The effect of this is a non-deterministic time gap between arrival of *Write* and reading of data in the receiver. Let T_R be the clock period of the receiver. Then the time gap between *Write* arrives till the data is actually read is in the interval [0, T_R] with uniformly distributed probability. Therefore, the data may be received sometimes correctly and sometimes erroneously when a delay fault exists in the data lines (Fig. 8a,b).

Let t_l be the time from the data arrives till the signal *Write* arrives at the receiver. The probability density function of t_l is expected to follow the distribution shown in Fig. 9. If t_l is positive (interval 3 in Fig. 9) there is no delay fault that causes erroneous data. If t_l has a lower value than $-T_R$, (interval 1 in Fig. 9) it means that a delay fault is present that always makes data erroneous. If t_l is between $-T_R$ and 0 (interval 2 in Fig. 9) the transferred data are received sometimes erroneously and sometimes correctly.

The basic idea of the proposed conservative test application method is to read the data one clock cycle before it is read under normal operation. Then the test consists of the transmitter sending data many times (say *m* times) with a long or random time gap between two data transfers. It can be shown that if the expected data is received correctly even once in *m* trials then the link is delay fault free. After *m* tests, the chip is marked MIGHT_BE_FAULTY, if for all tests the received signal was faulty. It is shown that the probability of declaring a good chip as faulty decreases exponentially with increase in *m*, which is illustrated by Table 3. Therefore, there is a very little chance to mistakenly classify a good link as faulty.

Table 3. Probabilities of declaring a good chip as faulty

t_l/T_R	10 %	1 %	0.1 %	0.01 %
≥1	1	1	1	1
0.99	1	1	2	2
0.9	1	2	3	4
0.5	4	7	10	14
0.1	22	44	66	88

Since, each data line can have two delay faults; one when it changes from 0 to 1 and the other when it changes from 1 to 0, then both transitions have to be tested. In fact, the signal dependency and fault detection conditions are rather more complicated in case of crosstalk. A special conservative but very effective fault model, called Maximum Aggressor fault model was proposed in literature for crosstalk testing. The model divides the link wires into two groups: one is victim and all others are aggressors with respect to the victim. Fig. 10 illustrates this principle. In the table, *i*-th signal is the victim and the patterns represent a complete crosstalk test set (6 patterns) for one victim.

Sequence

Bit positions in the bus			
i … i - 1	i	i + 1 … N	
000…000	0	000…000	Glitch test 1
111…111	0	111…111	
111…111	1	111…111	Glitch test 2
000…000	1	000…000	Skew test 1
111…111	0	111…111	Skew test 2
000…000	1	000…000	

Fig. 10 Test sequence for one victim

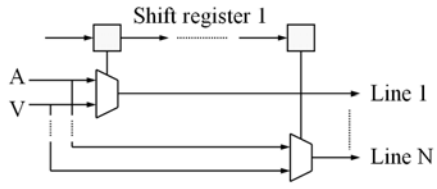

Fig. 11 Simple test generation HW

Since this fault model is conservative and therefore pessimistic in many cases, it is possible to relax it by allowing more than one victim to be simultaneously present in the link under test.

The test generation (TG) hardware illustrated in Fig. 11 allows for TG scheme to be reconfigured in the range from the most conservative and slow one to more relaxed but much faster one. This brings a freedom of test generation scheme selection to a test engineer at any stage of product development, production and test (both at the factory and in the field). This is another result of our current research in the area of interconnect testing.

A novel Boundary Scan-like Built-In Self-Test (BIST) conception for autonomous at-speed testing and diagnosis of interconnect was developed. It is based on a very efficient design of test pattern generation and response analysis hardware, which allows detection and diagnosis of both static and dynamic faults upon interconnects between chips in a multi-chip environment. The advantages of the new idea were demonstrated over other known methods. It was also shown that the new paradigm brings a never achieved before high level of universality, scalability, and configuration independence into the at-speed interconnect testing and diagnosis of interconnect.

New results:

Two new methods for at-speed testing of on-chip buses were proposed.

1. The first method is a test application and fault detection scheme that targets the asynchronous nature of NoC links where a Globally Asynchronous Locally Synchronous (GALS) operation principle is utilized. This scheme is the first of its kind available in literature [43].
2. The second method represents a flexible programmable embedded test pattern generation solution that supports a tradeoff between test speed and test quality and is designed for multi-layer on-chip bus structures [47].

Both methods primarily target delay faults and harmful interference due to crosstalk, where the second one is an improvement of the Maximum Agressor crosstalk model.

3. A novel Boundary Scan-like Built-In Self-Test (BIST) conception for autonomous at-speed testing and diagnosis of interconnect was developed [28,30,33]. The new paradigm brings a never achieved before high level of universality, scalability, and configuration independence into the at-speed interconnect testing and diagnosis of interconnect.

2.7. Fault Simulation Accelerator with Reconfigurable Hardware

Fault simulation is the most often used way of digital analysis and there exist many techniques to speed up simulation[1]. Efficient fault simulation algorithms for combinational circuits are known already for decades. However, it is the large sequential designs whose fault grading run times could be measured in years that drive the need faster implementation, e.g. by hardware emulation. At the same time, reconfigurable hardware, e.g., FPGAs, has been found useful as system-modeling environments[2]. This has been made possible by the availability of multi-million-gate FPGAs. For academic purposes, cheaper devices with rather large capacity, e.g., new Spartan devices, can be used.

The availability of large devices allows implementing not only the circuit under test with fault models but also test vector generator and result analysis circuits on a single reconfigurable

[1] P. McGeer, K. McMillan, A. Saldanha, A. Sangiovanni-Vincetelli, P. Scaglia, "Fast Discrete Function Evaluation Using Decision Diagrams." Proc. of ICCAD'95, pp.402-407, Nov. 1995.
[2] "Axis Systems Uses World's Largest FPGAs from Xilinx to Deliver Most Efficient Verification System in the Industry." Xilinx Press Release #0273 - http://www.xilinx.com/

device. To study the possibility of replacing fault simulation with emulation, we first had to solve some essential issues - how to represent logic faults in a synthesizable circuit, how to feed the test vectors into the circuit, and how to read and/or analyze the results of emulation? Then we created the experimental environment and performed experiments with some benchmark circuits. The experiments showed that for circuits and/or applications that require large numbers of test vectors, it is beneficial to replace simulation with emulation. More work is needed to integrate the hardware part with the software part of the test generation environment. In addition to merely increasing the speed of fault simulation, the idea proposed in this paper can be used for selecting optimal Built-In Self-Test (BIST) structures.

The emulation environment (Fig. 12) was designed to work together with Turbo Tester (TT) is a diagnostic software package developed at the Department of Computer Engineering of Tallinn University of Technology[3]. The main novelty of the emulation approach lies in implementing MUXes and a decoder for fault injection which, unlike the shift register based injection, allows to insert faults in arbitrary order. This feature is highly useful when applying the presented environment in emulating the test generation process. In addition, we use an on-chip input pattern generator as opposed to loading the simulation stimuli from the host computer. For the first series of experiments, we looked at combinational circuits only. Results of experiments with combinational circuits were presented in [7].

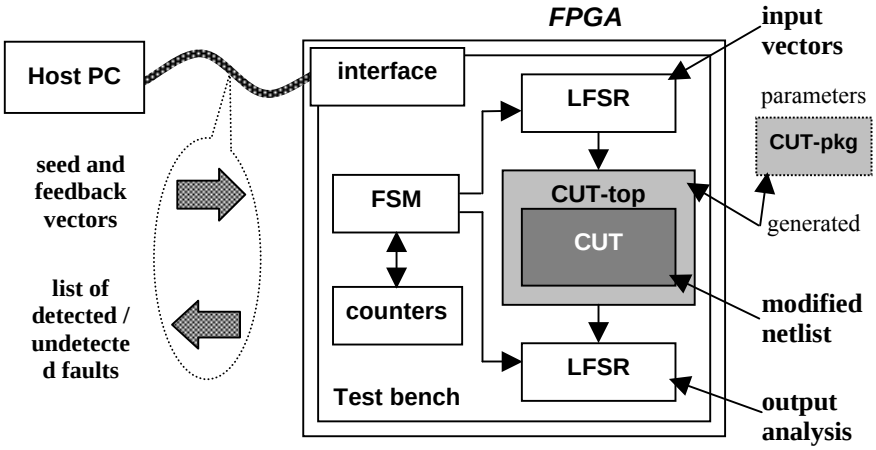

Fig.12. Emulation environment structure

For sequential circuits, most of the solutions used for combinational circuits could be exploited. The main modification was an extra loop in the controller because sequential circuits require not a single input combination but a sequence consisting of tens or even hundreds of input combinations. Also, instead of hard-coded test sequence generators and output analyzers, loadable modules were introduced [76]. To speed up simulation of sequential circuits, an approach with fault dropping was introduced [36]. Before building the experimental environment, we had first to solve how to insert faults, how to generate test vectors, how to analyze output data, and how to automate design flow.

The main problem in fault insertion was how to represent non-logic features - faults - in such a way that they can be synthesized using standard logic synthesis tools. Since most of the analysis is done using stuck-at-one and stuck-at-zero fault models, the solution was obvious - use multiplexers at fault points to introduce logic one or zero, or pass through intact logic

[3] "Turbo Tester" home page - URL: http://www.pld.ttu.ee/tt/

value. The extra multiplexers will increase gate count and will make the circuit slower (typically 5 to 10 times). For test vector generation and output data analysis, a well-known solution for BIST - Linear Feedback Shift Register (LFSR) - is used both for input vector generation and output correctness analysis[4]. LFSRs structures are thoroughly studied and their implementation in hardware is very simple. This simplifies data exchange with the software part - only seed and feedback polynomial vectors are needed to get a desired behavior. Output correctness analysis hardware needs first to store the expected output signature and then to report to the software part whether the modeled fault was detected or not.

For experiments, a powerful RC1000-PPE board with VirtexE chip (19200 slices) was used. Test circuits were selected from ISCAS'89 and HLSynt'92 benchmark sets to evaluate the speedup when replacing fault simulation with emulation on FPGA. For different benchmarks, the initial hardware emulation was in average 33 (ranging from 13 to 85) times faster than the software fault simulation. The improved environment was in average 250 times faster (from 44 to 517). It should be noted that when considering also synthesis times, it might not be useful to replace simulation with emulation, especially for smaller designs. Nevertheless, taking into account that sequential circuits, as opposed to combinational ones, have much longer test sequences, the use of emulation will pay off. This makes fault emulation very useful to select the best generator/analyzer structures for BIST. Another useful application of fault emulation would be genetic algorithms of test pattern generation where also large numbers of test vectors are analyzed. Future work includes development of more advanced on chip test vector generators and analyzers. [7,36,76]

New results:

1. A very fast approach to emulate fault simulation of sequential circuits on FPGAs was developed [36,76]. Compared to SW based solutions the speed of fault simulation increased more than 200 times.
2. Two alternative approaches were analyzed which can be considered as trade-offs in terms of required FPGA resources and fault grading accuracy. In addition, an environment for reconfigurable hardware emulation of fault simulation was proposed.
3. Experiments showed that it is beneficial to use emulation for circuits/methods that require large numbers of test vectors, e.g. simulation-based test pattern generation or validation.

2.8. Design for Testability

A comprehensive analysis of different approaches to increase the speed of test generation by improving testability has been carried out. As a result, a new DD based unified approach for calculating mixed-level testability measures was developed and experimented, and a new coarse-grain method was proposed for test point insertion at higher register transfer levels [78].

The method relies on inserting testability components to the RTL VHDL description of the design. The approach is based on non-classical, simplified concept of controllability and observability. The insertion takes place based on the list of uncontrollable and unobservable faults obtained by a sequential ATPG. Such interaction with an ATPG and resynthesis of the device after each test structure insertion would be very time-consuming. The proposed method solves its task with just three iterations. First, a testability analysis is carried out and controllability structures are inserted to the modules containing uncontrollable faults. Then,

[4] D.K. Pradhan, C. Liu, K. Chakraborty, "EBIST: A Novel Test Generator with Built in Fault Detection Capability." Proc. of DATE'03, pp. 224-229, March 2003.

the circuit is resynthesized and the ATPG is run. Second, the observability structures are added to the modules, with remaining unobservable faults. Finally, after resynthesis and an ATPG run the overhead area is minimized by removing observability structures from blocks, where there was no increase in fault coverage. A synthesizable VHDL library of dedicated generic components for testability structures has been implemented.

Experimental research with good results was carried out for RTL abstractions. Based on the new testability measures, a new advanced testability guided Register Transfer Level (RTL) Automated Test Pattern Generation (ATPG) for sequential circuits was developed [1,82].

The previous known methods have been implemented in test synthesis and in guiding gate-level test generation. However, works on application of testability measures to guide high-level test generation are missing. Experiments showed that testability measures greatly influence the fault coverage in RTL test generation with the proposed approach achieving the best results. The high-level testability measures were used for improving the testability of digital systems by inserting high-level control points [78].

The research on design for testability has been carried out in a close cooperation with Stockholm Royal Institute of Technology in Sweden.

New results:

1. A new high-level method for test point insertion for improving the testability of digital systems was developed [78].
2. New high-level testability measures were proposed, and using these measures for guiding the ATPG, the speed of test generation was considerably increased [1,82].

2.9. Design and Test Research Environment

The experimental tools developed in frame of the project formed the basis on which an integrated design and test research environment was created (Fig.13).

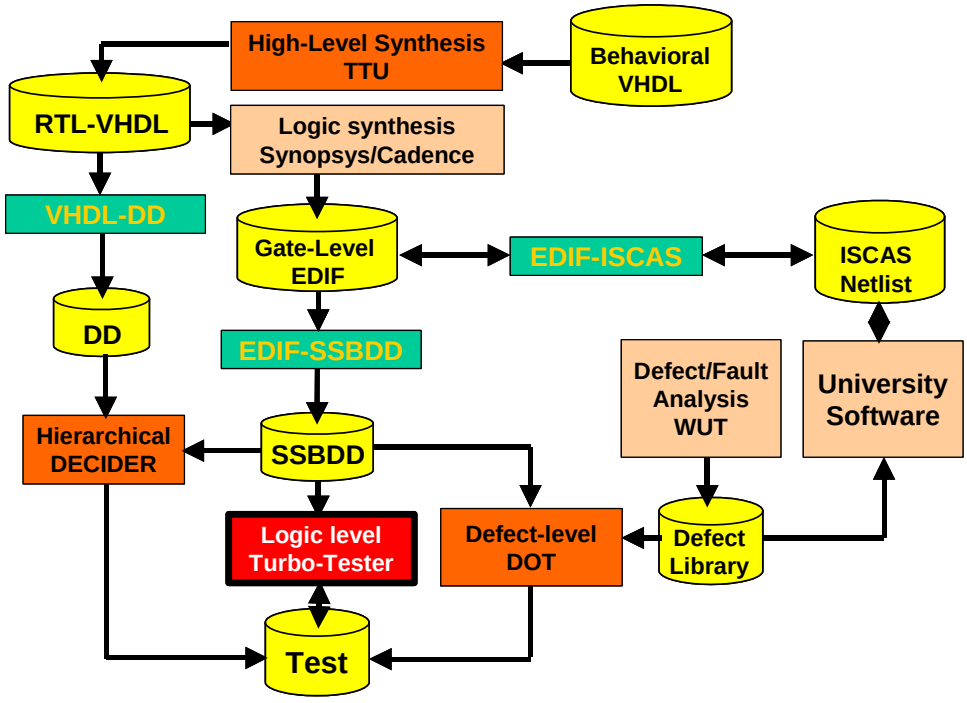

Figure 13. Hierarchical design and test research environment

The environment consists of the following parts (groups of tools):

- Synthesis tools (high-level and logic level synthesis)
- Test generation tools (hierarchical, logic and defect level test generators)
- Converters (interfaces between tools)
- Other (university) tools linked to the environment.

Design information can be created in different ways, i.e. by VHDL files to be processed by commercial or experimental high-level or logic synthesis systems, or created manually by schematic editors. The gate-level design is presented in the EDIF format. In university research practice, ISCAS benchmark families which have their own presentation format (ISCAS format) are widely used. In order to link test generation and fault simulation tools with all the needed formats, different converters are developed. EDIF netlists can be converted into ISCAS'85 or ISCAS'89 formats. Necessary technology library files to support such conversion have been created for the research environment.

The Turbo-Tester tools are based on Structurally Synthesized BDDs (SSBDD) they need EDIF-SSBDD to link the tools with commercial CAD systems. Hierarchical ATPG DECIDER uses two inputs – higher level (RTL) descriptions in VHDL and gate-level descriptions in EDIF. For importing VHDL descriptions to DECIDER which uses high-level decision diagrams (DD) as input, a converter VHDL-DD was developed.

As a set of examples, the following design flows can be exercised in this environment.

1. An RTL VHDL design is synthesized by high-level synthesis tool. A logic level synthesis for the high-level blocks follows. For these designs DD and SSBDD models are generated. Using DDs and SSBDDs, hierarchical ATPG DECIDER generates test sequences.
2. Using SSBDDs, Turbo Tester ATPG generates logic level test patterns targeted to detect logic level stuck-at faults.
3. Using SSBDDs and the defect library, the defect-oriented test generator DOT generates test patterns targeted to defect physical defects. The defect libraries available are created in cooperation with Warsaw University of Technology.
4. University tools that traditionally use ISCAS benchmarks can be linked via EDIF-ISCAS converter to commercial design tools that produce EDIF format.

Turbo Tester tool set represents an independent logic level test research environment (Fig.14). The Turbo Tester ATPG software consists of a set of tools for solving different test related tasks by different methods and algorithms:

- Test pattern generation by deterministic, random and genetic algorithms
- Test optimization (test compaction)
- Fault simulation and fault grading for combinational and sequential circuits
- Defect-oriented fault simulation and test generation
- Multi-valued simulation for detecting hazards and analyzing dynamic behaviour of circuits
- Testability analysis and fault diagnosis.

All the Turbo Tester tools operate on the model of Structurally Synthesized Binary Decision Diagrams (SSBDD). The tools of Turbo Tester run on the structural level. Two possibilities are available – gate-level and macro-level. In the latter case, the gate network is transformed into macro network where each macro represents a tree-like sub-network. Using the macro-level helps to reduce the complexity of the model and to improve the performance of tools. The fault model used in the Turbo Tester is the traditional stuck-at one. However, the fault simulator and test generator can be run also in the defect-oriented mode, where defects in the

library components can be taken into account. In this case, additional input information is needed about defects in the form of defect tables for the library components.

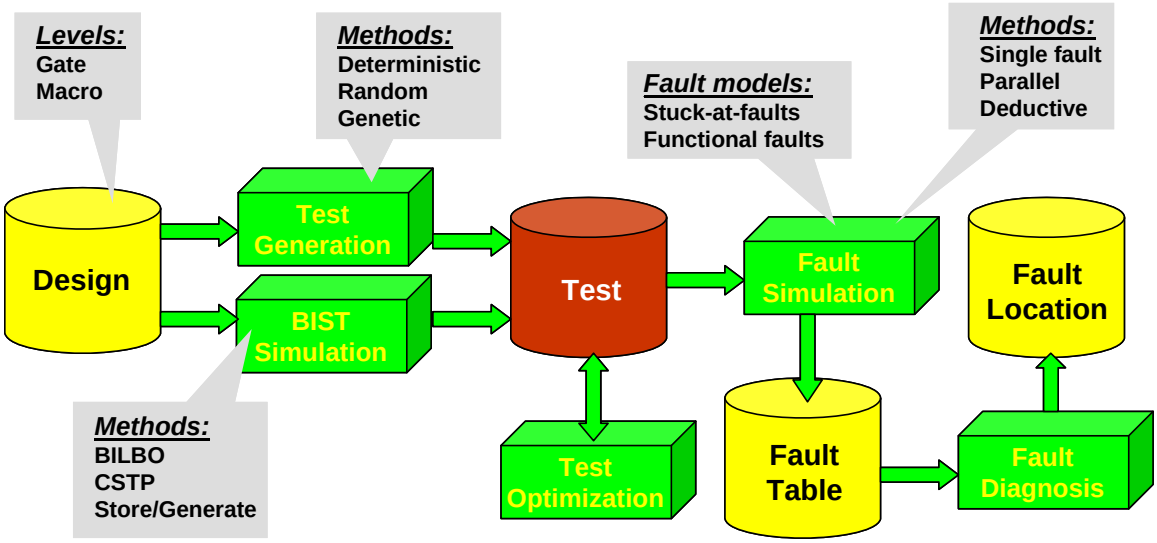

Figure 14. Logic level test research environment

The new quality and originality of the environment developed in the project is in the property of multi-functionality of the system (important for research and training), low-cost and ease of use. The multi-functionality means that different abstraction level models can be easily synthesized and resynthesized (to analyze the influence of the complexity of the model to the efficiency of methods), the methods are implemented by different algorithms (to analyze the efficiency of different approaches), the fault models can be easily changed and updated (to analyze the adequacy and accuracy of testing). The multi-functionality allows to set up and modify easily different experimental schemes and scenarios for investigating new ideas and methods.

The multi-functionality gives an excellent opportunity for students working in this environment to understand the ideas, advantages and drawbacks of different methods at changeable conditions. In traditional commercial design tools these purely research oriented possibilities are missing.

Most of the experimental research work carried out in the project was based on this environment. Thanks to this environment an intensive international research cooperation is continuously going on. Subcontractors of the project Fraunhofer Institute in Germany, Linköping University in Sweden, and Technical University Ilmenau have been one group of partners taking actively part in the development and in using this environment. Other partners have been: Warsaw University of Technology in Poland, Slovak Academy of Sciences, TU Darmstadt in Germany, Royal University of Technology Stockholm and University of Jönköping in Sweden a.o.

2.10. E-Learning Environment for Web-Based Study of Testing

The main goal of the conducted work was the creation of a homogeneous e-learning environment for studying the test and diagnostics of digital systems. In the end, the environment should consist of several interrelated and completed modules shown in Figure 3.

Some of the mentioned modules were partially available; some became implemented during this reporting period, while some others are still to be created or further improved.

The Turbo Tester

The engine [101] of the whole concept consists of PC-based tools installed locally and Java applets invoked remotely via Internet. The PC-based tool set was developed at TTU and it is called the Turbo Tester (TT) [14]. We selected TT for our environment because its range of compatible diagnostic tools forms, via their interaction and complementary operation, a homogeneous research environment, which provides good possibilities for laboratory training and experimental research.

The Java applets

The general idea behind the Java applets is a bit different. They are mainly aimed at supporting the concept of game-like style of learning via easy action and reaction, learning by doing, and concentration on most important topics in the simplest possible way. There are three different applets being by now almost ready and having their beta-testing stage running[1]. During the reporting period two of them were updated with new examples and functionality. The fourth applet, which represents a simple schematic and decision diagram (DD) editor, was started and it is currently under development. We tried to design our applets in a uniform way; so that the user once got acquainted with the overall style does not have to spend his time learning the new one again from the beginning.

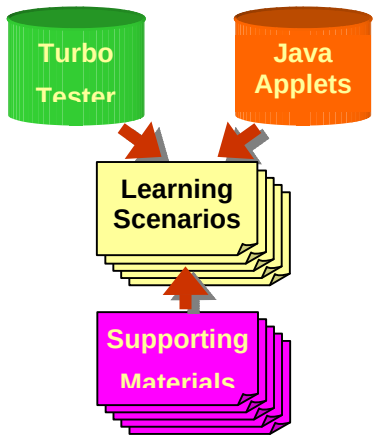

Fig. 15. Overview of the e-learning environment

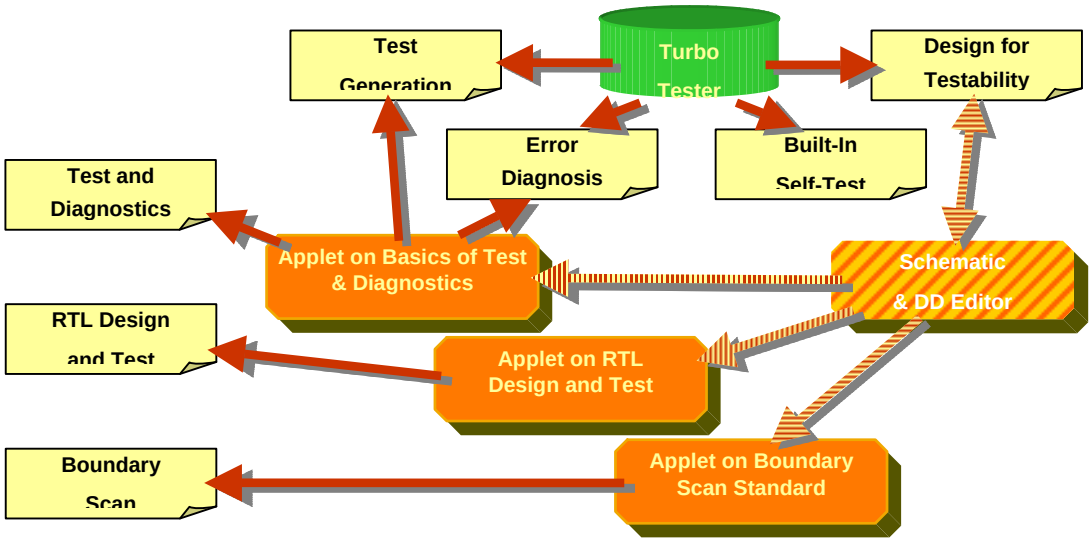

Fig. 16 Relationship between the applets, TT, and research scenarios

[1] Java applets home page: http://www.pld.ttu.ee/applets

The learning scenarios

The central point of the presented concept is a set of learning scenarios, which describe problems and experiments and represent virtual laboratory works, where students learn diagnostic software and get acquainted with common concepts and problems of testing and diagnostics. There are scenarios for beginners and for advanced study. The user-friendly graphical environment created by the applets is the best option for beginners. More advanced study is possible with scenarios, which make use of TT tools.

The general structure

Figure 16 represents an overall structure of relations between the applets, the Turbo Tester, and the learning scenarios. As it is seen from the figure, the advanced scenarios make use of both the TT and the applets. We call them laboratory works[2] since they are usually run in a class equipped with computers having Turbo Tester tools preinstalled. These scenarios were developed in the frames of previous projects and they got incorporated into this new environment. Another group of scenarios, called exercises, were developed during the reporting period. They are better adapted to self-study since together with the corresponding applets they represent platform-independent self-contained systems aimed at teaching target area of knowledge and engineering. Each of the two groups of scenarios should normally be used independently of each other, since there is some overlapping of studied topics.

Another important part of the environment embraces all kinds of supporting materials like user's manuals, help, theoretical reference material, etc. It was substantially updated during the reporting period. In the following, a short description of the applet-based scenarios is given. At the same time, this description covers also the functionality of the related applets. The full text of the scenarios is available in the Web[3].

Basics of logic level testing and diagnostics

This work introduces the very basics of logic-level digital test and diagnosis. Students start with fault sensitization and propagation and justification of signals. First, they learn how to generate a test vector for a particular fault. Then, they continue test generation for all the faults in a given simple circuit. When the test is ready, the task it to minimize the number of test vectors keeping the fault coverage on the same level. Students learn to compare the quality of different test sets. A pseudo-random test sequence is used as a reference here. During test generation, students understand the process of fault simulation and the conception of fault table. They learn to find and distinguish easy and hard-to-test faults. The fault diagnosis considered in the work is of two different kinds. The first one is the sequential diagnosis represented by guided probe technique. The other one is the combinational diagnosis based on fault table.

RTL design and test

Register Transfer level of digital system representation brings a lot of different conceptions to be taught to modern students. We are trying to cover some important topics of RT level design and test in our learning scenario. As in a real electronics system production cycle, the specification of the system comes first. In the current scenario, a certain algorithm, which has to be implemented by a student, plays the role of the specification. The student has to implement different versions of the same algorithm. Each version should meet some specific

[2] Laboratory training URL: http://www.pld.ttu.ee/testing/labs
[3] http://www.pld.ttu.ee/applets/td/td_exercises.html
http://www.pld.ttu.ee/applets/rtl/rtl_exercises.html
http://www.pld.ttu.ee/applets/bs/bs_exercises.htm

design requirement, like low hardware cost or high speed of operation. Students should select a proper structure of the datapath and write a microprogram, which represents the controller. The design validation and verification come next. This is done via simulation at different input data. At the same time, the speed of device operation can be measured. The hardware cost is primarily defined by used datapath resources. The testing for manufacturing defects is the next step of the product life cycle. We use different techniques of test generation (TG) and compare them in our scenario. Since the logic-level TG is considered in previous scenario, we do not pay much attention on it. However, we still give students possibility for revising their high-level test generation attempts on the logic level and for generation of additional test vectors if needed. Among the high-level test methods we single out such generic approaches as Functional Test and Functional BIST (F-BIST). Both methods are based on selection of proper operands in order to get good fault coverage. At this time, the device is working in its normal mode and simultaneously tests itself. The F-BIST technique allows insertion of additional control points for better testability. There are also another two BIST modes: Logic BIST, which is similar to BILBO and Circular BIST, which is analogous to CSTP.

Boundary scan standard

The BS standard is a very important state-of-the-art testing technique of modern complex integrated systems. The main goal of the work is to introduce the concept of Boundary Scan to students. They should learn the BS instructions and working modes and see from inside how the BS structures are operating. According to the standard, all the chips on the board are connected into a scan chain via TDI (Test Data In) and TDO (Test Data Out) pins. Hence, all the instructions and test data can be inserted via the single TDI input only. Therefore, the task of controlling the system of several BS chips is not a trivial one. First of all, students should study the Test Access Port (TAP) Controller, which is the key device in the whole BS conception. They learn to move from state to state on the state diagram and insert different BS instructions via TDI. The next step is the study of data registers and their proper usage. When the main principles of BS operation are understood, the students face the task of interconnect diagnosis. They should learn how to properly select test vectors in order to find interconnect defects of a given type. The final and the most advanced task is to write a description of an own chip according to given parameters using BSDL format.

The conception presented here is suitable for a broad audience of learners who are interested in studying different concepts of testing and diagnostics of integrated digital circuits.

3. COOPERATION WITH INDUSTRY

3.1. Cooperation with local industry

In Estonia the group has cooperational links to the following industrial companies: Artec Design, Elcoteq Network Corp., Analog Design AS, Liewenthal, Elvior, M&T Electronics, Cybernetica AS, Borthwick Pignon, AS MicroLink, National Semiconductor Estonia, Testset, Testonica Lab. For these companies our group has regularly organized tutorials or seminars either by the prominent experts from Western countries (Finland, Germany, UK, France etc.) and by the experts of our group.

A close cooperation between TTU and Estonian SME Artec Design (the subcontractor of TTU in WP4) has continued during the last three years. In the framework of this co-operation TTU has transferred its know-how on digital test to the design process of the company [69]. The company has been participated in developing the course materials for TTU.

A new built-in self-test concept has been developed and experimented in System-on-Chip design [48,59]. The new tools developed include software for emulating built-in self-test architectures [20,22,35,95] and tools for hierarchical fault simulation and test pattern generation [54,55].

During the project we had a placement of the group member Jaan Raik in Artec Design.

As a result of the project eVikings II, the Competence Centre of Mission Critical Embedded Systems (ELIKO) has been created (with contracts between 7 private companies and 2 research institutions under the leadership of TTU). Research group runs currently two joint projects with the company Artec Design.

As a result of the project also a new company Testonica Lab was recently created based on the know-how developed in this project.

A close research in the field of Binary Decision Dieagrams is carried out between matematicians of University Tartu and engineers of Technical University Tallinn. A definition of a new class of structurally synthesized BDDs was developed and several new properties of SSBDDs were defined [61,67]. These properies allowed to optimize SSBDDs and to reach higher speed in fault simulation.

3.2. Cooperation with industry outside Estonia

Outside Estonia the group has cooperational links to the following industrial companies: Ericsson AB, SAAB, and DIGSIM DATA AB in Sweden, JTAG Technologies and National Instruments in Sweden, Fraunhofer Institute of Integrated Circuits in Germany, and Insight Memex/Xilinx in France.

Industrial companies Ericsson AB and SAAB in Sweden are strongly interested in the competence of our group and in using it for developing new tools for supporting new

Boundary Scan standards, which are still under the development. This interest is based on our demonstration of the tools we have developed for modeling Boundary Scan processes at different conferences [28,30,33,34,53,85,87,]. Two presentations on these tools have been assigned the **Best Paper Award** [34,87].

Currently, the negotiations to set up a contract between TTU, Testonica Lab, Ericsson and SAAB are going on.

A tight cooperation has taken place between our group and the Fraunhofer Institute of Integrated Circuits in Dresden (Germany), which has been devoted to building up an internet based collaborative design and test environment.

In this cooperation the ATPG tool DECIDER developed at TTU has been adapted to the design flow used in the industry, and excellent results have been achieved in using the ATPG for several industrial designs. For example, it has been shown that the functional test for Huffmann decoder used in the industry had very low fault coverage (less than 20%). The fault coverage for this module was considerably improved by using DECIDER (up to 60%). Suggestions were developed for improving the testability of the module to reach further increase in the fault coverage.

A novel environment for an Internet-based co-operation in the field of design and test of digital systems has been developed in cooperation with Fraunhofer Institute (Germany). The test tools developed by our group can be run at geographically different places under the virtual environment MOSCITO developed in Germany.

As the result of this cooperation, 2 joint papers were published [62, 91].

In cooperation with DIGSIM DATA AB (Linköping, Sweden) a tool exchange has taken place. The diagnostic tool set Turbo Tester developed at TTU was used for teaching industrial engineers in Sweden on one hand, and the design environment DIXIcad developed in the company is being used in the educational environment at TTU for carrying out laboratory works for more than 100 students per year. DIGSIM DATA AB has also carried out a tutorial for students and engineers in Estonia.

JTAG Technologies and National Instruments in Finland have carried out twice a course on Boundary Scan Technology. One of our lab members Dr. Artur Jutman participated in these courses as a lecturer. JTAG Technologies was interested in the Boundary Scan applet developed by our group and expressed the wish to use this applet in their courses. Some extensions are being developed in this applet according to suggestions of JTAG Technologies.

4. ACADEMIC INTERNATIONAL COOPERATION

WP4 has cooperated with more than 20 academic institutions from 11 countries (USA, Germany, Sweden, Denmark, Czech Republic, Slovakia, Poland, Bulgaria, Russia, Ukraina and Byelorussia).

Especially intensive was collaboration with subcontractors: Fraunhofer Institute of Integrated Circuits in Dresden, TU Ilmenau (Germany) and Linköping University (Sweden) which resulted in 28 joint publications. In total, 50 joint papers were written with 35 researchers from 18 academic institutionsof 11 countries (the total number of paers published in WP3 was 105).

4.1. TU Ilmenau, Germany (Subcontractor S16)

Cooperative work with Technical University of Ilmenau (Germany) had the goal to develop new conceptions, methods and tools for internet based higher education in the field of design and test. The results are published in joint papers [34, 41, 42, 51, 53, 57, 66, 74, 75, 81, 89, 100, 103]. Further joint publications are currently being prepared.

The following students were sent to TU Ilmenau for a placement for 1-3 months: A.Jutman, S.Devadze, V.Rosin, R.Gorjachov, A.Chernov, J.Smahtina, N.Mazurova and A.Sergejev.

The results of the placements of our students at TU Ilmenau are as follows:

- Register Transfer Level Design and Test applet was developed, and the library of components was created (responsible for this work were S.Devadze, N.Mazurova, J.Smahtina). The address of the web site is: http://www.pld.ttu.ee/applets/rtl/.
- The Boundary scan applet was developed and equipped with a lot of working modes (responsible for this work were A.Jutman and V. Rosin). The address of the web site is: http://www.pld.ttu.ee/applets/bs/.
- An educational web site was developed where a lot of applets, exercises, laboratory works and corresponding theory on digital design and test has got reviewed, updated and reorganized (responsible for this work were A.Jutman and V. Rosin). The address of the web site is: http://www.pld.ttu.ee/applets/index.html#testing

The educational environment developed jointly support university courses on digital electronics, computer hardware, testing and design for testability to learn by hands-on exercises how to generate test patterns, and how to analyze their quality. The tasks chosen for hands-on training represent simultaneously real research problems, which allow to foster in students critical thinking, problem solving skills and creativity

In this cooperation other institutions took also part resulting in joint publications:

- Institute of Integrated Circuits of Slovak Academy of Sciences, Slovakia
- TU Sofia, Bulgaria
- Warsaw University of Technology, Poland
- Vladimir State Technical University, Russia
- Lviv Polytecnic National University, Ukraine
- Belorussian State University of Informatics and Radioelectronics
- Belorussian State University

4.2. Fraunhofer Institute of Integrated Circuits (Subcontractor S15)

A novel environment for an Internet-based co-operation in the field of design and test of digital systems was jointly developed. The test tools created by our group can be run at geographically different places under the virtual environment MOSCITO developed in Germany.

The following students had the placement in this institution: E.Ivask, J,Raik, A.Jutman.

As the result of this cooperation, 2 joint papers were published [62, 91].

4.3. Linköping University, Sweden (Subcontractor S14)

The topic of cooperation is research and development of new architectures of hybrid BIST for digital systems, formulating and solving optimizational tasks for test processes under the criteria like minimization of test time, peak power and energy consumption, memory requirements and and area overhead and improving the test quality and fault coverage.

Joint research with Linköping University has resulted in a series of papers on the emerging field of built-in self-test of SoC [5, 21, 22, 26, 35, 50, 52, 60, 77, 95-97], and further joint publications are currently being prepared.

4.4. Tomsk State University

The topic of cooperation is joint research on the model of Binary Decision Diagrams (BDD), and especially investigation of the properties of Structurally Synthesized BDD-s with the goal to use these properties for improving the efficiency of logic level test generation algorithms. Two joint papers were published [3,4].

4.5. Donetsk State University

The topic of cooperation is investigation of evolutionary approaches to test generation for functional BIST is considered. Several methods of deriving deterministic test sets at functional level were investigated, and one of them was implemented. Experimental data showed the efficiency of the proposed method [29,70].

4.6. Jönköping University

The joint research topic is interconnect testing in System-on-Chips and Networks-on-Chips with special interest of crosstalk errors. Testing of chips built using deep sub-micron technology is becoming harder since crosstalk and small variations in the fabrication processes are adversely affecting circuit dynamic behaviour. We have developed a conservative method that has the property that it can detect all faulty chips but may also label some good chips as faulty with a small probability [43]. It is possible to extend our method to combine it with functional testing of the link and adapt it for on-line testing. Another method and the corresponding BIST hardware were developed for at-speed testing of crosstalks [47]. The proposed BIST hardware is programmable and can provide the trade-off between test speed and test quality.

4.7. Kharkow National University of Radioelectronics

The main cooperation activity with KNURE is joint organization of the annual IEEE East-West Design & Test Workshops to bring together scientists from East and West. The workshop has taken place already 3 times in 2003-2005. They have been successful events and attracted more then 60-70 participants annually. The first workshop organized in the frame of this project in

September 2003 had a great success and got high interest from IEEE Computer Society and the Test Technology Technical Committee (TTTC) [8]. Now the conference has the IEEE label [11].

4.8. Stockholm Royal University of Technology, Sweden

The cooperation topics are different aspects of developing methods for designing digital systems. In design for testability field a new method for high-level testability measuring were developed [78]. A co-author V.Govind from KTH defended at TTU his MSc thesis, and he will continue in Tallinn also his PhD study. A cooperation is carried out also in the field of design of asynchronous circuits [49].

4.9. Defect-oriented testing

In this topic the cooperation has taken place between:

- TU Darmstadt, Germany
- University of Technology Warsaw, Poland
- Institute of Informatics of the Slovak Academy of Sciences, Slovakia

A new defect-oriented hierarchical approach for testing complex deep-submicron circuits was developed [15,17]. A defect-oriented deterministic test generation tool was developed (DOT). It was shown that 100% stuck-at fault tests covered only about 80-90% physical defects. The main feature of the new tool is its ability to reach 100% defect efficiency for the given set of defects by proving the redundancy of not detected defects. The tool allows to prove the redundancy of physical defects in relation to the logic behaviour of a circuit. Such a function of the tool to our knowledge in unique in the world [27,37,38].

4.10. Fault simulation

In this topic the cooperation has taken place between:

- Engineering College of Copenhagen, Denmark
- Aldec, Las Vegas, USA
- Kharkov National University of Radioelectronics

New approaches to deductive fault simulation were jointly developed with V.Hahanov (Ukraine) and S.Hyduke (USA) [12,93]. Method allows to increase fault simulation speed. A new method for hierarchical fault simulation of digital systems was jointly developed with B.Klüver from Denmark [86]. The approach proposed allows to reduce simulation cost in comparison to traditional gate-level fault simulation methods.

4.11. Other cooperation

In cooperation with researchers of many countries (Sweden, Italy, Spain and Estonia) a joint book was written on system level test and validation of HW/SW systems [21,22]. A textbook to support teaching test an testability issues was written with researchers from Czech Republik, Slovakia, Poland, Russia and Estonia [16]. The book includes also the educational tools on a CD developed jointly by TTU and TU Ilmenau [19,20].

4.12. Guest seminars and tutorials

The following seminars and tutorials were carried out by prominent western scientists and researchers at TU tallinn where a lot of bachelor, master and PhD students were involved together with participants from the Estonian industry:

1. **M.Austin** (JTAG Technologies, Finland), May 15, 2003
   Title: Boundary Scan Principles
2. **J.Pauve** (Insight Memex/Xilinx, France), May 15, 2003
   Title: Enhancing Board Testing Using Programmable Logic
3. **J.Palola** (National Instruments Finland), May 15, 2003
   Title: Configurable I/O with FPGA
4. **B.Bennetts** (Bennetts Associates, UK), Oct. 6-8, 2003
   Title: Techniques For Designing Testable ICs
5. **R.Hartenstein** (Kaiserslautern University, Germany), May 13.-16, 2004.
   Title: Reconfigurable Computing and its impact on embedded systems and supercomputing.
6. **K. Chakrabarthy** (Duke University, USA), September 10, 2004
   Title: Droplet-Based "Digital" Microfluidic Systems: Computer-Aided Design, Testing, and Applications
7. **T. Vierhaus** (Technical University of Brandenburg, Cotbus, Germany), Sept. 20-22, 2004.
   Title: Fault-tolerant systems
8. **H.Tenhunen** (KTH, Stockholm, Sweden), October 4, 2004
   Title: Educational Challenges and Strategies in Electronics
9. **M.Glesner** (TU Darmstadt, Germany), October 4, 2004
   Title: System Design Challenges in Ubiquitous Computing Environments
10. **S.Kumar** (Jönköping University, Sweden), October 5, 2004
    Title: Networks on Chip (NoC): a new paradigm for SoC Design
11. **B.Magnhagen** (DIGSIM DATA AB, Linköping, Sweden), October 6, 2004
    Title: Electrical test is not enough
12. **A.Zakrevski** (Academy of Sciences, Minsk, Belorussia), December 11-12, 2004
    Title: Discrete Systems
13. **Y.Zorian** (Virage Logic, USA), May 22, 2005
    Title: System on Chip: Embedded Test in Practice
14. **J.L.Huertas** (IMSE-CNM, Spain), May 22, 2005
    Title: Design for Test of Analogue and Mixed-Signal Integrated Circuits
15. **J.Segura** (Balearic Islands University, Spain), May 24, 2005
    Title: Understanding Failure Mechanisms and Test Methods in Nanometer Technologies
16. **P.Maxwell** (Agilent Technologies, USA), May 24, 2005
    Title: CMOS Image Sensors and Optical Testing
17. **H.-J.Wunderlich** (University of Stuttgart, Germany), May 25, 2005
    Title: From Embedded Test to Embedded Diagnosis
18. **H.G.Kerkhoff** (Institute for Nanotechnology – The Netherland), May 25, 2005
    Title: Testing of MEMS-based Microsystems
19. **D.Borrione** (Fourier University Grenoble), June 3-5, 2005
    Title: Formal verification of digital integrated systems
20. **P.Amblard** (TIMA Laboratory, Grenoble), June 3-5, 2005
    Title: Design of finite state machines

Conclusions

The joint research work described above had a goal to strengthen international co-operation in the domain of digital systems, to develop new contacts with international research community. The research activity of TTU has found international recognition by winning the competition for organizing one of the most important test events in the World – IEEE European Test Symposium, which was held in Tallinn in 2005.

5. DISSEMINATION OF RESULTS

The results of WP4 have been disseminated at different events, seminars and courses, organized by WP4 or carried out by active participation of WP4 team (presentations on conferences and workshops are excluded from this list):

1. Presentation of chapters of the course of "Digital Test" (D4.1) in the Tutorial "Defect-Oriented Testing of Digital Systems" at the Lviv Polytechnic National University, Lviv, **Ukraine**, February 17, 2003, organized in the framework of the EU project IST-2000-30193 REASON.
2. Hands-on course "System Verification and Test" (5 weeks) based on chapters of the courses of "Digital Test", "Design for Testability" (D4.1) and courses on DDs and SoC Testing (D4.5) with lectures (24 h) and lab work (12 h) in frame of the International Master School at Jönköping University, **Sweden**, January 25 – March 1, 2003.
3. Presentation of chapters of the course "Design for Testability" as invited tutorial in frame of the 3-day Training Course "Digital Systems Testing and Design for Testability" at the Linköping University, **Sweden**, March 19-21, organized in the framework of the EU project IST-2001-35100 SYDIC-Training.
4. Presentation of a chapter on Testing of NoC as an invited 4-hour tutorial in frame of series of tutorials on "Networks on Chips" at the University of Technology Stockholm, **Sweden**, May 19, carried out by the authors of the book "Networks on Chip", edited by A.Jantsch, H.Tenhunen. Kluwer Academic Publishers, 2003.
5. Presentation of a chapter on Boundary Scan technique of the course "Design for Testability" (D4.1) as invited lecture in the frame of the international 1-day tutorial "Boundary-Scan Seminar: Facing Challenges in Board Level Testing", organized by TTU in **Tallinn** on May 15, 2003.
6. Presentation of chapters of all the mentioned new courses (D4.1 and D4.5) in the 2-day tutorial "Design and Test of Digital Circuits", organized by TTU in **Tallinn** on May 20-21, 2003.
7. Lecture "Distance learning tools for the field of Digital Testing" related to hands-on courses of "Digital Test" and "Design for Testability" (D4.1) in frame of the Tutorial "Defect-Oriented Testing of Digital Systems" in Liberec, **Czech Republic**, June 2, 2003.
8. Hands-on course "Design for Testability" (1 week) with lectures (24 h) and lab work (8 h) based on the courses of D4.1 held in frame of the Microelectronics Summer School at TU Darmstadt, **Germany**, Aug. 11-30, 2003.
9. Hands-on session "E-learning environment for digital test: Applets and PC-based tools" given in the Testing Tools Workshop in Bratislava, **Slovakia,** September 11, 2003.
10. Presentation of chapters of the course on SoC Testing (D4.5) in the Tutorial "Defect-Oriented Test of Integrated Circuits and Systems" in connection with the 4th Electronic Circuits and Systems Conference in Bratislava, **Slovakia**, September 12, 2003, organized

in the framework of the EU project IST-2000-30193 REASON.

11. The 1st East West Design & Test Workshop - EWD&TW'03 organized by TU Tallinn in Alushta, **Ukraine**, on September 17-21 in a cooperation with local organizers – Kharkow National University of Radioelectronics (KNURE).
12. Tutorial "Advanced Methods for Defect-Oriented Testing of Digital Systems" held in the frame of EWD&TW'03 in Alushta, **Ukraine,** on September 19-20. Chapters of the course "Digital Test" (D4.1) were presented.
13. Invited lecture "Digital Test in Estonia" (*venia legendi*) at the Kharkow National University of Radioelectronics, Kharkow, **Ukraine**, September 22, 2003, held by Raimund Ubar, as elected Professor Honoris Causa of KNURE.
14. In October 5, 2003, a 30-minute overview of HLS related issues was given for computer science PhD students participating Estonian Computer Science seminar in Pedaste, **Estonia**. The number of participants - 34 (not all were students).
15. In the frame of the joint project of Nordic and Baltic Countries "SoC Technologies for SMEs" supported by Nordisk Industrifond, a seminar was organized by TTU in **Tallinn** on October 13 with the goal to introduce to the local SMEs the possibilities of SoC design.
16. Design for Test Seminar organized by TTU with cooperation of JTAG Technologies, Finland in **Tallinn** on October 21, 2003.
17. Presentation of chapters of the courses on DDs and SoC Testing (D4.5) in the Tutorial "Advanced Methods for Defects Testing" at the TU Sofia, **Bulgaria**, October 25, 2003, organized in the framework of the EU project IST-2000-30193 REASON.
18. Hands-on course "System Verification and Test" (5 weeks) based on chapters of the courses of "Digital Test", "Design for Testability" (D4.1) and courses on DDs and SoC Testing (D4.5) with lectures (24 h) and lab work (12 h) in frame of the International Master School at Jönköping University, **Sweden**, January 19 – March 4, 2004. Participants: 24 students.
19. Lecture course (12h) "Test Generation and Fault Simulation in Digital Systems" at the Kharkov National University of Radioelectronics, **Ukraine**, April 6-8, 2004. Lecturers: R.Ubar (TTU). Participants: 120 students, 10 teachers.
20. Tutorial (4h) in connection with the Conference DDECS 2004 in Stara Lesna, **Slovakia**. Title: Defect Oriented Test Generation. April 18, 2004. Organizer IISAS. Lecturers: M.Renovell (LIRMM, France, guest lecturer), W.Pleskacs (WUT, Poland), V.Stopjakova (TUS, Slovakia), R.Ubar (TTU). Participants: 45 (students, teachers, engineers).
21. Tutorial (4h) in connection with the Conference DDECS 2004 in Stara Lesna, **Slovakia**. Title: Additional Hardware for IC Testability Improvement. April 18, 2004. Organizer IISAS. Lecturers: O.Novak, Z.Pliva (TULC, Czech Rep), Z.Kotasek (TU Brno, Czech Rep), A.Jutman (TTU). Participants: 45 (students, teachers, engineers).
22. Tutorial (6h) in Sofia, **Bulgaria**. Title: Advanced Methods of Testing Electronics Systems. May 29, 2004. *Organizers:* TU Sofia and **TU Tallinn**. *Lecturers:* W.Pleskacs (WUT, Poland), V.Stopjakova (TUS, Slovakia), R.Ubar (TTU), Z.Pliva (TU Liberec, Czech Rep.). Participants: 25 (students, teachers, engineers).
23. Tutorial (3h) in connection with the International Conference MIXDES 2004 in Szczecin, **Poland**. Title: Methods of Testing of Electronics Systems. June 25, 2004. *Organizer:* **TU Tallinn.** *Lecturers:* R.Ubar (TTU), R.Sheinauskas (TU Kaunas, Lithuania), S.Mosin (TU Vladimir, Russia). Participants: 10 (students, teachers, engineers).

24. Tutorial (6h) in Tomsk, **Russia**. Title: Advanced Methods of Digital and Analog Test. September 6, 2004. *Organizers:* TU Tomsk and **TU Tallinn**. *Lecturers:* D.Wuttke (TU Ilmenau, Germany), W.Pleskacs, W. Kuzmicz, E.Piwowarska (WUT, Poland), V.Stopjakova (TUS, Slovakia), S.Mosin (TU Vladimir, Russia), R.Ubar (TTU). Participants: 40 (students, teachers, engineers).
25. Tutorial (6h) in connection with the International Conference ICAM 2004 in Irkutsk, **Russia**. Title: Advanced Methods of Digital and Analog Test. September 10, 2004. *Organizers:* TU Tomsk and **TU Tallinn.** *Lecturers:* D.Wuttke (TU Ilmenau, Germany), W.Pleskacs, W. Kuzmicz, E.Piwowarska (WUT, Poland), S.Mosin (TU Vladimir, Russia), R.Ubar (TTU). Participants: 50 (students, teachers, engineers).
26. Tutorial (6h) in Vladivostok, **Russia**. Title: Advanced Methods of Digital and Analog Test. September 13, 2004. *Organizer:* TU Vladivostok and **TU Tallinn**. *Lecturers:* D.Wuttke (TU Ilmenau, Germany), W.Pleskacs, W. Kuzmicz, E.Piwowarska (WUT, Poland), V.Stopjakova (TUS, Slovakia), S.Mosin (TU Vladimir, Russia), R.Ubar (TTU). Participants: 20 (students, teachers, engineers).
27. Tutorial (2h) in connection with the Summer School "System-on-Chip - SOC'04" in Smolenice, **Slovakia**. Title: Hierarchical defect-oriented test generation. Sept. 21, 2004. *Organizer:* ISAS Bratislava, Slovakia. *Lecturer:* **R.Ubar (TTU).** Participants: 35 (students, teachers, engineers).
28. Tutorials (6h) in connection with the Autumn School "Advanced Methods for Systems-on-Chip for Ambient Intelligence" in Sinaia, **Romania**. Titles: 1. Code Transformations and Hardware Synthesis. *Lecturer:* **P.Ellervee (TTU).** 2. Hierarchical Test Approaches for Digital Systems. *Lecturer:* **R.Ubar (TTU).** Oct. 9, 2004. *Organizer:* TU Bucharest, Romania. Participants: 15 (students, teachers, engineers).
29. Lecture course (32h) "Design for Testability" in connection with the International Microelectronics Summer School at TU Darmstadt, **Germany**, October 11-16, 2004. *Lecturers:* **R.Ubar, A.Jutman (TTU).** *Organizer:* TU Darmstadt, Germany. Participants: 12 master students.
30. Tutorial (1,5 h) in connection with the International Conference DLESC 2004 in Minsk, **Belarus**. Title: Hierarchical Test Generation in Digital Systems. November 12, 2004. *Organizer:* BSU Minsk. *Lecturer:* **R.Ubar (TTU).** Participants: 40 (students, teachers, engineers).
31. Hands-on course "System Verification and Test" (6 weeks) with lectures (24 h) and lab work (12 h) in frame of the International Master School at Jönköping University, **Sweden**, January 20 – March 15, 2005. Organizers: Jönköping University and TTU. Lecturers: R.Ubar, A.Jutman (TTU). Participants: 19 students.
32. Tutorial (2h) in connection with the Conference DDECS 2004 in Sopron, **Hungary**. Title: Why we need deterministic test pattern generation? April 13, 20045 Organizer TTU and TU Budapest. Lecturers: R.Ubar (TTU), A.Jutman (TTU), O.Novak (TU Liberec, Czech Republic), E.Gramatova (IISAS, Slovakia), V.Stopjakova (TUS, Slovakia). Participants: 25 (students, teachers, engineers).

6. SELF-EVALUATION OF THE PROJECT RESULTS

Tallinn University of Technology was the leader of WP4. The project was extremely useful, since it provided a remarkable support to the research, development of new courses and creating a laboratory environment, and to maintaining international contacts by sending our students to other universities and by welcoming at our university guest researchers and professors from other universities.

Initiated by the development opportunities generated by this project as well as by other international cooperation and domestic activities, two new competence centers were established as the result of the project at the Tallinn University of Technology

- Research Centre for Dependable Computing (CDC), and
- Development Centre of Mission Critical Embedded Systems (ELIKO) with contracts between 7 private SMEs and 2 research institutions under the leadership of TTU.

Both of these centers are working on transfer of technology to the SME-s influencing the technology development of the local industry. Through ELIKO very tight links have been established now between the Academia and the industry of Estonia.

As the result of this project and gathered know-how a new small company was recently established – Testonica Lab. Industrial companies Ericsson AB and SAAB in Sweden are strongly interested in the competence of our group. Currently, the negotiations to set up a contract between TTU, Testonica Lab, Ericsson and SAAB are going on.

As the result of intensive international cooperation several new joint research directions were launched: defect-oriented digital testing, built-in self-test in digital systems, and development of new e-learning tools and teaching methodologies. The new research results and new teaching and learning conceptions developed during the last three years have been presented at international conferences and published in scientific journals. The total number of the project related publications are – 105. Half of them (50) are joint papers with 35 colleagues abroad from more than 10 countries. This fact demonstrates a really tight and productive international cooperation set up thanks to the project.

This research has leaded to creation of many new professional SW tools to support design and test of digital systems, which has been integrated into a new high-level research and teaching environment.

The project has had a very strong impact in improving the level of teaching. Four new courses have been developed in frame of WP4 of the project and have received a broad international recognition. The courses have been introduced not only into the curricula of TU Tallinn, but have been taught also in other leading universities in Europe. For example, the courses of Digital Test and Design for Testability have been carried three times at the TU Darmstadt (Germany) and three times at the University of Jönköping (Sweden). This cooperation will

continue in the next years. Based on these new courses during the project 30 tutorials, seminars or lectures have been carried out in more than 10 universities in Europe, and also in connection with different high-level conferences. The educational tool set developed in frame of the project has been downloaded in more than 90 universities in about 30 different countries. This large network will have a high potential for us for the future cooperation not only in education but also in research. Negotiations towards joint research are ongoing with different companies in Europe like Fraunhofer Institutes in Germany and Ericsson AB and SAAB in Sweden.

The created new laboratory environment allows effective teaching of the developed courses, and continuation of the already well running collaboration between us and our international partners in research. To make the cooperation and joint research easier, most of the developed tools can be used remotely via Internet.

One of the most important consequences of the project was to stimulate creation of interfaces between our tools and our international partners' tools, which has resulted now in the end of the project in a broad virtual laboratory, and in a lot of synergy via integrating the competences, know-how and experiences of different partners.

7. FULL DESCRIPTION OF DELIVERABLES

All the deliverables can be found in: http://www.pld.ttu.ee/~raiub/eVikings/

D4.1 (Month 20). Development of 2 hands-on courses

Two hands-on courses were planned and developed (the first course was completed in the first project year, the second one in the second year):

- Course "Digital Test" (D4.1a);
- Course "Design for Testability" (D4.1b)

*Digital Test (Deliverable **D4.1a**)*

The course gives an overview of methods, algorithms and models used for testing digital systems. The main topics of the course are: introduction to digital test, mathematical basics (Boolean differentials and decision diagrams), fault modeling and fault properties, test generation for different types of systems (combinational and sequential circuits, memories, microprocessors), universal test sets, random and pseudorandom tests, fault simulation and test quality analysis, fault diagnosis and fault localization.

The hands-on part of the course consists of two lab works:

- *Test generation.* Learning basic principles of test generation via manual test pattern composition for a small combinational circuit, analysis of fault simulation data, and practicing with automatic test pattern generators and comparison of different approaches via estimation of the test quality.
- *Error diagnosis.* Learning the difference between the manufacturing and the diagnostic tests, basic concepts of diagnosis through composition of diagnostic patterns for a simple circuit, and localization of a wrong gate inside the suspected faulty area of the circuit.

The course material is presented on:
http://www.pld.ttu.ee/~raiub/web_0103/diagnostika/loengukiled/

*Design for testability (Deliverable **D4.1b**)*

The course gives an overview of methods, algorithms and models used for design for testability (DFT) of digital systems. The main topics of the course are: quality policy of electronic design, tradeoffs of DFT, testability measures, calculation of signal probabilities, ad hoc rules for DFT, scan-path design methodologies, Boundary Scan standard, synthesis of testable circuits, built-in self-test (BIST), test generation in BIST, response compaction in BIST, BIST implementation and architectures, hybrid BIST, functional hybrid BIST, IEEE 1500 standard.

The hands-on part of the course consists of two lab works:

- *Design for testability.* Learning basic principles how to measure the testability features like controllability and observability, how to improve the testability by inserting control points, how to reduce the area overhead in DFT by multiplexing and demultiplexing inputs/outputs, time sharing of input/outputs, and how to improve the testability by using scan-path technique.
- *Built-in self-test.* Learning basic architectures of BIST, how to measure the quality of BIST, how to improve the fault coverage by combining pseudorandom patterns with stored deterministic patterns, and how to find optimal combinations of hybrid BIST.

The course material is presented on:
http://www.pld.ttu.ee/~raiub/web_0103/disain_ja_test/loengukiled/

D4.2 (Month 25). Organization of international workshops

Initially 3 international workshops were planned. In fact, the following 6 events (3 workshops, 1 conference and 1 symposium) were carried out:

- **D4.2a.** 1st East-West Design and Test Workshop – EWD&TW'03 was carried out by the main organization of TTU on September 17-21, 2003 in Alushta (Ukraine) in cooperation with local organizers – Kharkow National University of Radioelectronics (KNURE)[3];
- **D4.2b.** 2nd IEEE East-West Design and Test Workshop – EWD&TW'04 was carried out in Alushta on September 23-26, 2004 in cooperation with local organizers KNURE[4];
- **D4.2c.** 9th Baltic Electronics Conference – BEC'2004 was carried out by TTU on October 4-6 2004 in Tallinn;
- **D4.2d.** 10th IEEE European Test Symposium – ETS'05 in May 22-25, 2005 in Tallinn. A great success: 154 papers were submitted compared to about 100 in previous years. Only 31 papers were selected which guaranteed a very high level event. Two of the papers belonged to the researchers of TTU. The total number of participants was more than 200, which was also the record in the history of ETS. The WP4 leader as the General Chairman was awarded by IEEE Computer Society by the Meritorious Service Award (for providing the leadership to the ETS in the past decade and significant services as General Chair in 2005).
- **D4.2e.** 4th IEEE European Board test Workshop – EBTW'05 in May 25-26, 2005 in Tallinn. The workshop was also success with more than 50 participants.
- **D4.2f.** 3rd IEEE East West Design & Test Workshop in September 15-19, 2005 in Odessa in cooperation with local organizers KNURE. The number of participants was very high - 70.

D4.3. Publications

Originally 30 articles were planned. In fact, 105 papers in internationally reviewed journals, books and proceedings were published (15 journal papers, 3 books, 7 chapters in books) and 80 conference papers. The list of the publication is given also in the list of references in the

[3] V.Hahanov, R.Ubar. 1st East West Design&Test Workshop IEEE Design & Test, Nov.-Dec 2003, pp.103.
[4] V.Hahanov, R.Ubar. 2nd IEEE East West Design&Test Workshop. IEEE Design &Test, Nov.-Dec 2004, pp.594.

end of the report

D4.4 (Month 11). Semiconductor Technology, Design and Test Roadmap report

The report considers the main developments in semiconductor industry according to the leading roadmaps. System drivers, the main challenges in the design area and the trends in test methods, tools and the Automatic Test Equipment (ATE) are presented. The impact of the developments foreseen by The International Technology Roadmap for Semiconductors (ITRS) to the Estonian research community and industry in the microelectronics field is discussed.

D4.5 (Month 10). Studies on different topics

The studies on decision diagrams and logic level testing, methods for fault simulation for SoC-s, and methods for high-level synthesis were planned and as reports delivered

*Studies on Decision Diagrams and Logic Level Testing (Deliverable **D4.5a**)*

The course gives an overview about emerging mathematical tool of decision diagrams and of his use in the field of Digital Test. The main topics of the course are: Binary Decision Diagrams (BDD), Structurally Synthesized BDDs, synthesis and main properties of BDDs, comparison of SSBDDs with gate-level circuits, using SSBDDs for test generation, fault simulation and fault diagnosis, high-level DDs for representing digital systems at different levels: finite state machines, register transfer level, instruction set architectures, synthesis of DDs, using DDs for high-level and hierarchical test generation.

*Studies on Testing of Systems-on-Chip (Deliverable **D4.5b**)*

The complexity of Systems-on-Chip (SoC) and Networks-on-Chip (NoC) makes the application of traditional testing methods obsolete. Here, a combination of methods known from hierarchical testing of digital systems, memory test and FPGA test area should be used. These include functional test, full-scan test, logic BIST, RAM BIST and testing of interconnect switches and wires. In this report we first, introduce the general concepts of testing digital circuits and systems, i.e. fault modeling, fault simulation and test generation. Subsequently, we present the new trends in digital test that could be used in testing the SoC and NoC designs.

Two main trends to be discussed are the defect-oriented test and the hierarchical test. Both are caused by the increasing complexities of systems based on deep-submicron technologies. The complexity problems in testing digital systems are handled by raising the abstraction levels from gate to register-transfer, instruction set architecture and behavioral levels. On the other hand, to handle adequately the defects in circuits implemented in deep-submicron technologies, new fault models and defect-oriented test generation methods should be used. As the consequence of these two opposite trends hierarchical and defect-oriented approaches are emerging in testing complex digital systems. In this report we present a combined defect-oriented hierarchical approach to testing complex deep-submicron circuits.

Built-In Self-Test (BIST) is the main concept for testing the cores in systems on chip. In this report, logic BIST and RAM BIST will be described. In addition we propose new hybrid BIST schemes for BIST optimization. Hybrid BIST containing both hardware and software components is probably the most promising approach for testing the resource nodes of SoC.

Further, Design-for-Testability (DfT) issues of SoC will be discussed. In densely packaged

digital systems with embedded memories and reusable cores scan-based approaches are the most commonly used methods to improve the design testability. P1500 standard for core test, test access mechanisms, test control and isolation issues will be discussed as prospective methods for enhancing SoC testability. In addition, the task of testing the NoC interconnect switches and wires will be explained in the report.

*Testing Strategies for Systems-on-Chip of Systems-on-Chip (Deliverable **D4.5c**)*

Complexity problems in test generation and fault simulation for digital systems are handled by raising the abstraction levels from gate to higher system representation levels. On the other hand, the need of higher quality of testing today's submicron integrated circuits, defect orientation is gaining more and more attention. As the consequence of the two opposite trends today – defect orientation and high-level modeling - hierarchical approaches are emerging in the test field. The main topics of the course are: overview about defects, modeling defects by Boolean differential equations, mapping physical defects onto the logic level, the meaning of faults and test generation hierarchy, bottom-up and top-down approaches for hierarchical test generation, hierarchical fault simulation methods.

*High-Level Synthesis (Deliverable **D4.5d**)*

High-Level Synthesis (HLS) takes a specification of the functionality of a digital system and a set of constraints and finds a structure that implements the intended behavior and satisfies constraints. This eight-hour course gives an overview of tasks and methods used in HLS. The course starts with a description of synthesis tasks, reasons to use design automation, and benefits of HLS. Three main tasks of HLS (scheduling, resource allocation, and binding) are described in details together with example algorithms. The course ends with a small hands-on exercise where participants are expected to design a FIR filter starting from algorithm and producing its RT level architecture (with FSM). The course can be given in two ways - one day and two days. The longer version expects the lecturer to explain presented algorithms in more details. Also, the hands-on exercise is longer and includes modeling and synthesis of the filter. The course material has been tested in the events 6, 14, and 15 of the dissemination list.

All the four deliverables can be found in http://www.pld.ttu.ee/~raiub/eVikings/D4_05/

D4.6 (Month 29). Participation in international conferences

Originally 10 conferences were planned. In fact, 74 papers were presented at 34 conferences, 6 symposia and 10 workshops. 3 papers earned Best Paper Awards, twice we received invitations to present papers at plenary sessions. Statistical data about participation in conferences is presented in the Table.

Statistical data:

Year	Conferences		Symposia		Workshops		Best paper awards	Invited papers
	Number	Papers	Number	Papers	Number	Papers		
2005	10	17	1	4	2	3	1	1
2004	12	20	2	2	6	7	-	-
2003	9	12	3	3	2	2	2	1
2002	3	3	-	-	-	-	-	-

D4.7 (Months 14, 26). RTD reports reviewed by advisory board

The 1st Annual report was reviewed by 4 Advisory Board members:

- Prof. Zebo Peng, Linköping University, Sweden (08.04.2004)
- Prof. Bengt Magnhagen, Jönköping University, Sweden (24.04.2004)
- Prof. Manfred Glesner, TU Darmstadt, Dresden (29.04.2004)
- Prof. Günter Elst, Fraunhofer Institute of ICs, Dresden, Germany (12.05.2004)

The 2nd Annual report was reviewed by 3 Advisory Board members:

- Prof. Günter Elst, Fraunhofer Institute of ICs, Dresden, Germany (15.04.2004)
- Prof. Zebo Peng, Linköping University, Sweden (18.04.2004)
- Prof. Einar Aas, Norwegian University of Science and Technology, Norway

All reviews were positive.

D4.8 (Month 29). Presentations of Estonian RTD results in SoC

In total, 41 presentations were made about the Estonian research results directly in the field of design and test of Systems-on-Chip (24 presentations at different conferences, and 13 at different seminars and tutorials in 7 countries). The total number of disseminations of all the research results in WP4 was 106 (74 presentations on conferences, and 32 at different seminars and tutorials in 11 countries).

D4.9 (Month 29). Study visits of students

During the first project year the following study visits of students at the subcontractor-universities TU Ilmenau and University of Linköping were organized:

1. D4.9a. Artur Jutman (PhD student, 3 months at the TU Ilmenau, June-August, 2003) [13,17,18].

   The main activity: research on using Binary Decision Diagrams in Testing [22,29], and on development of the concept of e-learning in teaching Design and Test [28,34,36,44,49,52].

2. D4.9b. S. Devadze, T. Vassiljeva [22], J.Smahtina [19], N.Mazurova [19] (MSc students, each 1 month at the TU Ilmenau, August, 2003).

   The main activity: Development of applets for modeling test processes at the register transfer level.

3. D4.9c. M. Jenihhin (MSc student, 3 months at the Linköping University, April - June 2003) [4,10].

   The main activity: Research on the field of optimization of hybrid BIST processes.

During the second project year the following study visits of students at the subcontractor-universities TU Ilmenau and University of Linköping were organized:

4. D4.9d. Ahti Peder (PhD student from Tartu University, 4-months at the TTU, Oct 2003 - Jan 2004).
   The main activity: The goal of the visit was to strengthen of the cooperation in the fields of Boolean algebra and logic testing between two universities in Estonia – TU and TTU. Two papers were presented at the international conferences [22,29].

5. D4.9e. Vineeth Govind (MSc student from Royal Institute of Technology Stockholm, Jan-

April 2004).
The main activity: As the result of the visit was, new efficient high-level testability measuring methods for complex digital systems were developed. Based on this work he defended his master thesis at TU Tallinn. The results are published in [40].

6. D4.9f. Artur Jutman - PhD student, 2 months at the TU Ilmenau, July-August, 2004. The main activity: research on using Binary Decision Diagrams in Testing [22,29], and on development of the concept of e-learning in teaching Design and Test [28,34,36,44,49,52].
7. D4.9g. Sergei Devadze (PhD student, 2 months at the TU Ilmenau, July-August, 2004). The main activity: research on fault simulation in digital circuits and systems-on-chip [49].
8. D4.9h. Vjatsheslav Rosin (MSc student, 2 months at the TU Ilmenau, July-August, 2004). The main activity: development of e-learning tools on Boundary Scan Conception for teaching Design and Test of digital systems and SoC [52].
9. D4.9j. Tatjana Shchenova-Vassiljeva (MSc student, 4 months at the Linköping University, April - June, 2004).
The main activity: research on low-power BIST in SoC [50].
10. D4.9k. Joachim Sudbrock (MSc student from TU Darmstadt, Sept 2004 - Feb. 2005). The main activity: As the result of this visit he carried out a research in defect-oriented testing, and we developed jointly a defect-oriented deterministic test generator. Such a tool does not exist in the present moment in the world. Based on this work he defended his master thesis at TU Tallinn. The results are published in [48,51].

During the third project year the following study visits of students at the subcontractor-universities TU Ilmenau and University of Linköping were organized:

11. D4.9l. Sergei Devadze (PhD student, 2 months at the TU Ilmenau, July-August, 2005). The main activity: development of e-learning tools on Boundary Scan Conception for teaching Design and Test of digital systems and SoC.
12. D4.9m. Anton Chernov (BSc student, 2 months at the TU Ilmenau, July-August, 2005). The main activity: development of e-learning tools on modeling LFSR processes.
13. D4.9n. Andrei Sergejev. (BSc student, 2 months at the TU Ilmenau, July-August, 2005). The main activity: development of e-learning tools on minimization of Boolean functions
14. D4.9p. Albina Jutman. (BSc student, 2 months at the TU Ilmenau, July-August, 2005). The main activity: development of educational scenarios based on DefSim chip

PhD Thesis defended:

Artur Jutman "Selected Issues of Modelling, Verification and Testing of Digital Systems" (2004) Reviewers: Prof. M.Renovell, LIRMM, France; Prof. M.Glesner, TU Darmstadt, Germany.

D4.10 (Month 29). One practical placement in industry

1st project year:

The following two practical placements were organized in 2003:

1. Practical placement at SME Artec Design (Jaan Raik, January, 2003)

The main activity: During the practical placement the design group of Artec Design shared their knowledge about industry standards in System-on-Chip design. TTU's role was to

develop self-test solutions for the cores in Artec's new SoC product. As a result of the stay, two tools were developed.

- A parametrical Built-In Self-Test (BIST) simulation tool for embedded cores.
- A VCD interface for the TTU's fault simulation tool to be used for measuring the fault coverage of functional test.

In addition, a 30 page technical report (in Estonian) was prepared to document the use of TTU tools in digital design and test process.

2. Practical placement at the Fraunhofer Institute of Integrated Circuits in Germany (Eero Ivask, September, 2003)

The main activity: Purpose of practical placement in Fraunfofer IIS in Dresden was to gain their expert knowledge in the following aspects:

- Developing distributed web applications with Java servlets and applets
- Setting up and using Tomcat web server
- Practical experience using MySql with Java. Developing and managing Java projects with Integrated Development Environment (IDE) "Eclipse" for Java.
- Feedback and feasibility assessment for User Tracking Software System Requirements definition.
- Feedback and feasibility assessment for User Tracking Software System Specification documentation.

The goal was to promote and integrate programs from software package “Turbo Tester” (developed in Tallinn Technical University) into e-learning system under development in Fraunhofer IIS, to create software module for user tracking.

3rd project year:

During the second project year the following one practical placement was organized at the Fraunhofer Institute of Integrated Circuits in Germany:

3. Practical placement at the Fraunhofer Institute of Integrated Circuits in Germany (Eero Ivask, March, 2005)

   The main activity: The purpose of the stay was to improve the web-based access of Turbo-Tester tools via the MOSCITO environment. Also a grid computing solution for Turbo-Tester tools was worked out allowing running one task on several computing stations in parallel.

8. FUTURE PERSPECTIVES

Based on the multi-functional research environment developed in the project and a very intensive international cooperation, clear plans have been made for the future research and development activities. The plans target the following research fields:

- Defect-oriented testing
- Hybrid built-in self-test in systems-on-chips.
- Testing of networks-on-chips
- Reconfigurable logic
- Theory of Decision Diagrams
- Support software for new emerging Boundary Scan standards S-JTAG and I-JTAG
- e-Learning teaching environment

1. In defect-oriented testing the class of physical defects will be extended, corresponding research on modeling new fault types like opens, delays, crosstalking etc. will be carried out. Thereafter the functionality of the novel defect-oriented test generator DOT will be also extended towards new physical defect classes. The research will be carried out in cooperation with Warsaw University of Technology (Poland), Jönköping University (Sweden), TU Darmstadt (Dresden).
2. In hybrid BIST the set of criteria as restrictions or cost functions for optimization tasks will be extended. The new emerging problem of hybrid functional self-test will be attacked. The results of the research in this area will be directly implemented in SoC design at Artec Design Company. International cooperation partners will be Linköping University in Sweden and TU Darmstadt in Germany.
3. In the field of NoC testing new BIST algorithms and architectures will be developed for interconnect testing and for core testing. The cooperation partners will be Jönköping University (Sweden), TU Darmstadt (Dresden).
4. The research on creating fault simulation accelerators using reconfigurable logic will be continued. The range of tasks where we try to exploit the reconfigurable logic instead of software will be extended.
5. The cooperation with Tartu University in the field of theory of decision diagrams will be continued. New properties will be investigated and new more efficient methods for optimization of DDs will be developed.
6. The research on Boundary Scan conception, and the development of new testing methods based on Boundary Scan will be carried out. The results will be implemented in Artec Design (Estonia), Ericsson AB and SAAB (Sweden). In the development process Testonica Lab will take actively part.

7. Extension of the educational environment is planned in parallel with getting new research results and developing new tools for experimental research. In this way the lab level where the students are getting their practical experience will stay at the leading edge of knowledge. On the other hand the students are taking directly part in the process of creating new knowledges.

An interest exists at TU Darmstadt and University Jönköping to continue the course on testing that our group has carried out already the last three years. This course will be continuously updated, and a new course “Fault-tolerant systems” is under development.

The workshop EWD&TW will be again organized in 2006 in cooperation with KNURE (Ukraine), and increasing number of participants is expected. TTU is one of the candidates to be the host of the European Dependable Computing Conference in 2007.

The first part of the Test Book in Estonian was published this year. For the next two years the second and third parts are planned.

Three proposals were submitted to the call for FP6-2005-IST-5 STREP/STIP where the group of WP3 is one of the partners.

9. FINAL CONCLUSIONS

The general aim of the work package was to strengthen and support research and development activities in line with the MEDEA roadmap, particularly in design and test of digital systems, and implementation of new research results as innovative CAD tools in the local industry.

1. An intensive research in this WP was carried out in a broad field of digital design and test. New mathematical models, algorithms and methods were developed for fault modeling in digital systems, automatization of test generation, fault simulation and built-in self-testing. As the result of this research in the last 3 years 105 scientific papers were published (3 books, 15 journal papers, 7 chapters in books and 80 papers in conference proceedings).
2. The most valuable results based on this research can be summarized as follows:
   - A tool for proving redundancy of physical defects in digital circuits was created for the first time ever. This feature of the tool allows to evaluate the quality of test generation more adequately than the existing tools can do. The new tool allows to reach 100% defect coverage, which cannot be done with other existing tools since they are not equipped with defect coverage measurement function.
   - A new hierarchical automated test pattern generator (ATPG) for digital systems was developed. The new tool is faster and reaches the best fault coverage compared to the known university tools whereas commercial hierarchical ATPG tools are missing.
   - A very fast approach to emulate fault simulation of sequential circuits on FPGAs was developed. Compared to the SW based solutions the speed of fault simulation increased more than 200 times.
   - A new research direction was opened targeted to optimization of hybrid built-in self-test BIST processes and hybrid functional self-test processes. The core of this direction consists of a new fast cost estimation method for BIST and of a new iterative approach based on this method for optimization of complex BIST processes. An intensive future research is planned in this direction.
3. As a result of the research, a lot of prototype tools were created and combined in a multi-functional CAD environment that has been used both for research and teaching purposes. It was and is being used for several projects with Estonian industry.
4. New testing methodologies were developed and experimented in cooperation with company Artec Design, new BIST ideas are being developed and used for industrial purposes in the Development Centre ELIKO, new Boundary Scan and interconnect testing methods developed in the project will be now the content of the new industrial projects to be contracted with Testonica Lab in Estonia and with Ericsson AB and SAAB in Sweden.

5. A very important result of the project (with a lot of input from WP3) was creation of the following new institutions:
   - Development Centre of Mission Critical Embedded Systems (ELIKO) was created with contracts between 7 private companies and 2 research institutions under the leadership of TTU. Research group runs currently two joint projects with ELIKO and with the company Artec Design.
   - A new company Testonica Lab was recently created based on the know-how developed in this project. Currently, the negotiations to set up a contract between TTU, Testonica Lab, Ericsson and SAAB are going on.
6. The results obtained in the project (new research results, new prototype tools, multi-functional research environment available for international cooperation) have been disseminated intensively (at least on 74 conferences, and on 32 different seminars or tutorials in 11 countries.
7. WP4 has cooperated with more than 20 academic institutions from 11 countries (USA, Germany, Sweden, Denmark, Czech Republic, Slovakia, Poland, Bulgaria, Russia, Ukraina and Byelorussia), which has resulted in 50 joint papers with 35 researchers from 18 academic institutions. The diagnostic tool set Turbo Tester has been used in more than 90 institutions in about 30 countries.
8. The research results of WP4 are being used in the company Artec Design and in the development centre ELIKO in Estonia. A cooperation with about 10 other companies in Estonia had the form of organizing for them seminars or giving consultations. A contract with companies Ericsson AB and SAAB in Sweden and the Estonian company Testonica Lab are under negotiations. TTU is cooperating with DIGSIM DATA AB (Sweden) in a form of exchanging tools. About 100-150 students of TTU are using yearly the CAD system DIXIcad developed at DIGSIM. The diagnostic tools developed at TTU were used by DIGSIM in teaching Swedish design engineers.
9. The project gave a possibility to organize 18 placements of students for 1-3 months at different universities in Europe (3 placements in industry). Three students (2 from abroad and 1 from Tartu University) had placements at TTU and worked for WP4. We invited 20 guest lecturers, and we organized 6 international conferences or workshops.
10. The work in Workpackage 5 (two annual reports) has got 7 reviews from 5 members of the Advisory Board (from Sweden, Germany and Norway). The reviews were positive.

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