A Test Point Insertion Algorithm for Mixed-Signal Circuits

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Abstract

This paper presents an algorithm based on testability measurement for test point insertion of mixed-signal circuits. Two transfer function models compatible with analog models are proposed: one is for digital devices and the other is for A/D interface components. An industry power supply circuit and a common A/D converter circuit are used to validate our approaches.

1.0 Introduction

The rapid increase in mixed-signal applications has created interesting challenges in design and testing. The Design for Testability (DFT) technology should increase a system's testability resulting in improved quality while reducing test cost and time to market[1].

In the early stage of design, testability should be included. There are two schemes to improve the testability of a circuit. One is to redesign the circuit[2][3], while the other is to insert the test points[4] into the circuit. Each of these techniques has its own advantages. The right choice depends on the particular application.

Fast and effective techniques of testability analysis and test point insertion are important for designers to reduce the high cost of mixed-signal circuits. Test point insertion in digital circuits have been studied extensively[5]. For analog and mixed-signal circuits, test point insertion was presented in [6][7]. In these two papers, test point selection was developed based on a linear error model for analog and mixed-signal circuits. This work focused on selecting a subset of specification test points. While this guarantees correct specification, it does not ensure structural correctness. On two other papers [13][14], the topology of circuits is adopted to evaluate the circuit diagnosability. The rule of test points selection was to achieve the best diagnosability with minimum number of test points. A limitation of [13] was the assumption that the board was unpowered and all semiconductors were open. All branches were treated in equal weight in [14], which are not effective when the branches have differences in capability for voltage or current transformation.

In this paper we present a method for structural test point selection in mixed-signal circuits based on a behavior models of components. The objective of this method is to select a set of test points (nodes of a circuit) for enhancing structural testability without extensive fault simulation.

1.1 Testability measure

In [9] testability analysis of analog circuits was discussed. Testability is represented by two criteria: controllability and observability. These two criteria are defined below.

Controllability: Controllability measures the relative difficulty of setting the voltage or current of a node to a specific value.

Observability: Observability measures the relative difficulty of observing the current or voltage value of a node from primary outputs.

Testability is defined as geometric mean of controllability and observability.

Both controllability and observability are associated with nodes in a circuit. The components connected between these nodes are described by Testability Transfer Factor (TTF). The TTF of a component represents quantitated controllability and observability transfer between the inputs and outputs of the component. The TTF of a passive device is an impedance based measure shown as following:

$$TTF(z) = 1 - \frac{z(\omega)}{OC} \qquad (1.1.1)$$

where z is the impedance value of the component connecting two nodes, which is a function of frequency ω. *OC* is the open circuit resistance. A device with multiple inputs and outputs is described with a group of TTF values corresponding to each pair of input and output nodes. Active devices are also represented by a transient impedance network[9].

In this work, the method to analyze testability in mixed-signal circuits is developed using the same definition of TTF. The TTF of digital circuit was first derived by Stephenson and Grason[10]. It is a measure of how well a component transfers the test information between inputs and outputs.

Two factors, CTF (Controllability Transfer Factor) and OTF (Observability Transfer Factor), are employed for controllability and observability calculation. Digital TTF models have been studied extensively. Several digital testability analysis software packages have been developed (e.g., SCOAP[10], TMEAS[11] and CAMELOT[12]). Six variables were used to represent controllability and observability [10]. The authors of [11] used bus based models, whereas in [12] a signal value CTF for the whole component was adopted.

However, these models are incompatible with analog models discussed in [9]. We developed unified models with separate TTF values, from each input to each output.

1.2 Test points

Test points are nodes that are employed as control and observation points to enhance the testability of the whole circuit without changing the functionality of the circuit under test. There are three kinds of test points:

Control points are those nodes that can be re-configured with additional circuitry to become the primary inputs in order to increase the overall controllability of the circuit.

Observation points are those nodes that can be re-configured to become primary outputs to increase the observability of the circuit.

Test points are nodes which are both controllable and observable.

Although test point insertion does not change the functionality of the circuit, it does add some delay and noise to branches connected to the test points. It is crucial to select the test points so that their insertions have minimal effect on the circuit.

2.0 Test point insertion algorithm

Based on testability analysis, test points can be added to increase the overall testability. There are two strategies in test point insertion. One is to fix the number of test points then optimize testability. The other is to fix the threshold value of testability then minimize the number of test points. Figure 1 shows the test point insertion procedure in a flow chart.

In this paper, the circuit under test is described by a netlist, the initial state of the circuit, and a list of primary inputs and outputs. The testability before test point insertion is calculated using the initial state. Then the nodes are sorted according to their fan-in and fan-out TTF values. If a device has very low TTF value, it will reduce the testability transfer between its inputs and outputs. The controllability of the nodes connected to the outputs of such a device will be adversely affected. Similarly, the observability of the nodes connected to the inputs will degrade. Nodes that are outputs of low TTF value devices have greater potential to increase the overall controllability if re-configured as control points. The same applies to nodes that are inputs of low TTF value devices for increasing the observability. Nodes have large fan out can also improve the overall testability. Our sorting algorithm considers the above criteria. In our testability analysis algorithm, a circuit is represented by TTF matrices (i.e., control matrix and observation matrix). By using the matrices, contributions of fan in branches and fan out branches are included.

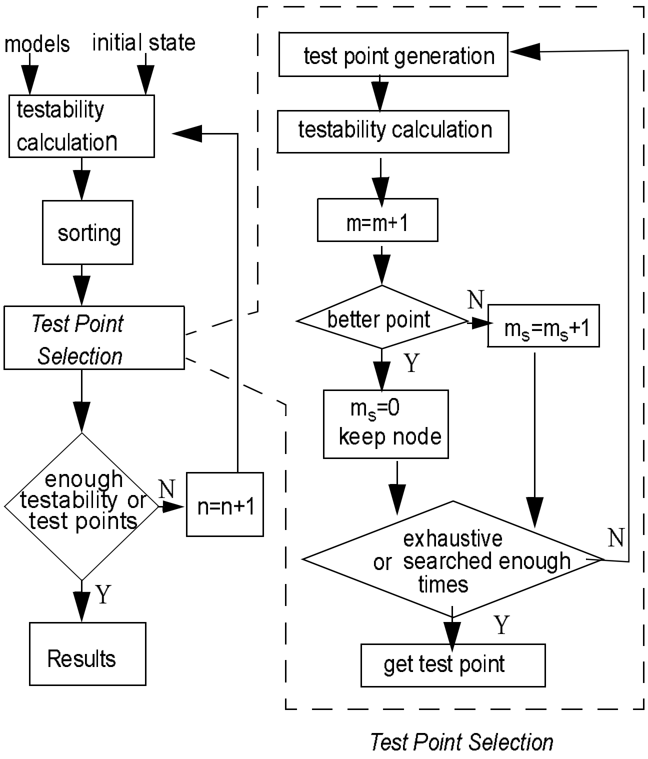
Take the control matrix (Cmatrix) as an example. Controllability of node i can be calculated from Equation (2.0.1)

$$C_i = \frac{1}{F_{in}} \sum_{j=1}^{N} C_j \bullet TTF_{ij} \qquad (2.0.1)$$

where C_i = controllability of node i

F_{in} = fan-in of node i

C_j = controllability at source node of fan-in



n = number of selected test points

m = number of searched nodes

m_s = the number search times

Figure 1:Test Point Insertion Algorithm

TTF_{ij} = TTF from node *i* to node *j,* element of Cmatirx

N = number of nodes

Summation of the *i*-th row of Cmatrix is the TTF value that node *i* gets from its fan-in nodes (denoted as *Ci-in*), whereas summation of the *i*-th column represents the fan-out condition of the node (denoted as *Ci-out*). Decreasing of *Ci-in* or increasing of *Ci-out* will increase the possibility of node *i* to be a control point. Therefore, the nodes are sorted in the descending order of the values subtracting *Ci-out* from *Ci-in*. Same algorithm is used with the observation matrix to obtain the search squeeze for observation points.

Test point search begins from the top point in the sequence. The selected node is re-configured as primary input or primary output or both according to its pre-defined type. After the re-configuration, the testability is re-evaluated and compared with the previous value. If it is greater than the previous one, the point is retained. Otherwise, pick the next point from the sequence. For a small circuits (less than 300 nodes), a full search is performed for each test point selection. For large circuits, each search stops when a node is selected or a given maximum number of points have been considered.

In this algorithm, the speed of testability evaluation is the decisive factor. Simple and effective hierarchical models can speed up the testability analysis.

3.0 TTF models

In our model, a uniform TTF for both controllability and observability transformation is presented. Controllability is propagated along the signal flow graph (SGF) and observability is propagated in the reverse direction of SGF. This TTF definition is exactly compatible with that of the analog model's in [9]. Thus the digital and analog components can be analyzed with same algorithm.

3.1 TTF of digital circuit

Our TTF model of digital gates is based on truth tables which is suitable for both basic gates and complex hierarchical circuits. In the derivation which follows, TTFs are represented as TTF_C (TTF of controllability) and TTF_O (TTF of observability). As proven below, they share the same value in our model.

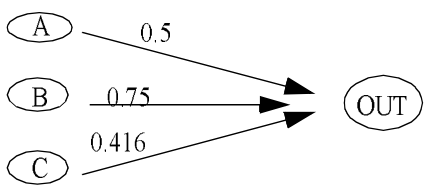


Figure 2: SGF of a complex gate

TTF_C is derived on how much each input can affect each output. Taking a pair of input and output, the output is represented by the maxterm and the minterm expressions corresponding to the truth table. If the output is to be set to “1”, any one term in the minterm expression can do. The shortest term including the given input will decide the controllability of this input to set this output. Similarly, the shortest term of the maxterm expression including the given input will decide the controllability of this input if the output is to be set to “0”. The TTF_C from this input to this output is the average of values to set the output to “1” and “0”.

TTF_O represents how much we can decide each input by observing each output. Again we represent the output by the maxterm and the minterm expressions. When the output is “1”, each term in maxterm expression must be one. Using the shortest term including the given input. we can determine the value of the input. When the output is “0”, the shortest term that has the given input in minterm expression will give out the value of observability of this input. Average value in these two conditions is the TTF_O from the this output to this input.

TTF_C and TTF_O are equal for each pair of input and output, then they are represented by a uniform TTF as in (3.1.1) and the signal flow direction is from input to output.

$$TTF_{in-out} = \frac{\frac{1}{n_{max}} + \frac{1}{n_{min}}}{2} \qquad (3.1.1)$$

where

n_{max} = number of variables of the shortest term containing the given input in the maxterm expression of *out.*

n_{min} = number of variables in the shortest term containing the given input in the minterm expression of *out.*

Following is an example:

$$OUT = AB + \bar{A}BC \qquad (3.1.2)$$

$$= (A + C)B \qquad (3.1.3)$$

As shown in Figure 2, TTF of B to OUT is the average of 0.5 and 1. The value 0.5 comes from the term AB in (3.1.2) and the value1 comes from term B in (3.1.3). Figure 2 is the SGF of this complex gate where TTF includes three values, one from each input to the output.

Using the same method, we can set up a testability library of basic digital gates and some special complex gates.

3.2 TTF of A/D interface component

In this section, we will discuss the TTF of an A/D interface component. Controllability from inputs to outputs will depend the input signals range to set a specific output value. Observability from output to input will be determined by the inputs' range which we can infer through observing outputs' values. A comparator is used as an example.

The comparator is one of the most popular A/D interface component. As shown in Figure 3, the analog input voltage is compared to the reference voltage and a two state output is obtained. Since the output takes only two values, we are mainly interested in "1" and "0" conditions.

In Figure 3, *output* will be set to "1" if V_{in} is in the range of "1" (V_{in} is larger than V_{ref}). *Output* can be reset to "0" by having V_{in} in the range of "0" (V_{in} is smaller than V_{ref}). Thus V_{ref} divides the all possible input voltage values into two ranges. If V_{ref}becomes larger, the range of "1" will shrink so we have less choice of V_{in} to set *output*. On the other hand, if V_{ref} is reduced towards V_l, the range of "0" will reduce so that resetting will be more difficult. The worst case is that V_{ref}equals to V_h or V_l, where the output value will be a fixed single value and will become uncontrollable by V_{in}. under this condition, controllability of V_{in} to *output* is zero. In general, when either becomes smaller, the controllability decreses. The mathematical expression is,

$$TTF = \frac{min((Vh - Vref), (Vref - Vl))}{Vh - Vl} \tag{3.2.1}$$

Rewriting equation (3.2.1):

$$TTF = \frac{1}{2}\left[1 - \frac{|Vref - Vm|}{Vm - Vl}\right] \tag{3.2.2}$$

For observability, since the comparator is a many to one mapping, a single value of the output corresponds to a range of input values. The smaller the range is, the easier it is to infer the input value. TTF is a function of reference voltage at given input range. This can be described as,

$$TTF = 1 - \frac{max((Vh - Vref), (Vref - Vl))}{Vh - Vl} \tag{3.2.3}$$

Rewriting (3.2.3), we get:

$$TTF = \frac{1}{2}\left[1 - \frac{|Vref - Vm|}{Vm - Vl}\right] \tag{3.2.4}$$

which is the same as (3.2.2).

TTF of analog components and the algorithm for testability analysis was presented in [9].

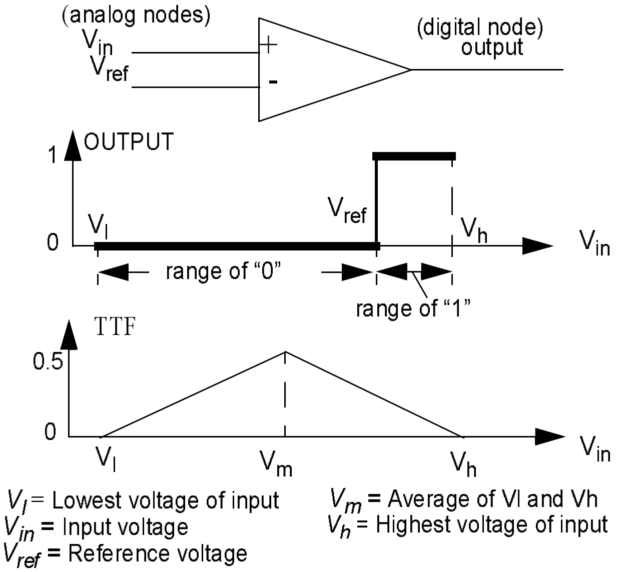


Figure 3: Comparator and its TTF

4.0 Result

The method presented previously is applied to two mixed-signal circuits: an industry power supply and a 4-bit successive- approximation ADC.

4.1 Power Supply

Power supply is a device to transfer AC power into DC power. The diagram is shown in Figure 4. The circuit under test includes resistors, inductors, capacitors, transformers, opto-couplers, buffers, flip-flops, pulse width modulator (PWM), power FETs, diodes, and opamps, etc.

Since test points add both area and performance overhead, it is important to minimize the number of test points. Using our technique, four test points to increase testability are selected. Table 1 shows the improvement in controllability, observability and testability.

To validate this research, the circuit designer was asked to select a set of test points without knowledge of our selection. The designer selected test points intuitively based on his knowledge of design and testing. Three out of the four points selected by our technique were included in the set of points selected by the designer. For a large circuit our tech-

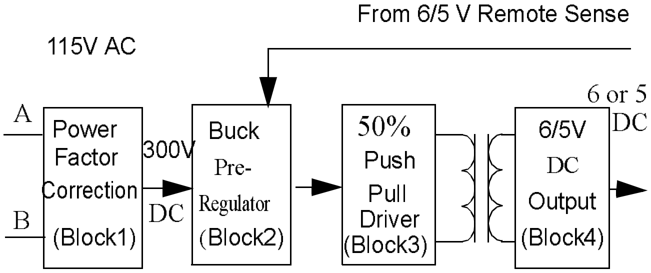

From 6/5 V Remote Sense
115V AC
A
B
Power Factor Correction (Block1)
300V DC
Buck Pre-Regulator (Block2)
50% Push Pull Driver (Block3)
6/5V DC Output (Block4)
6 or 5 DC

Figure4: Power Supply

nique provides a systematic methodology to assist the test point selection.

TABLE 1. Testability improvement

	0 test points	4 test points	improvement
controllability	0.3319	0.4571	36%
observability	0.4830	0.5888	20%
testability	0.3370	0.4995	48%

4.2 4-bit successive-approximation ADC

A 4-bit successive-approximation ADC is analyzed as another example. Its basic components are gates, D-flip-flops, CMOS switches, resistors, a comparator and an opamp. Figure 5 is the diagram of this ADC. The *Digital Encoder* is mainly composed by two groups of D-flip-flops. *DAC* structure is a reduced-resistance-ratio ladder with an opamp. A_{in} is the input analog voltage, *B0 to B3* are the outputs from MSB to LSB.

TABLE 2. Test Points and testability improvement

	before	after	improvement
4 control points controllability	0.506	0.732	31%
4 observation observability	0.125	0.541	331%
4 test points testability	0.181	0.439	142%

Three groups of test points are selected corresponding to the improvement in controllability, observability and testability. The results are shown in Table 2. *B0 to B3* control the ADC directly, an increase in their controllability will improve the overall controllability. The four control points are connected with the data and clock inputs of the output D-flip-flop group. They can increase the overall controllability by increasing the controllability of *B0 to B3*. As outputs, *B0 to B3* are totally observable. Because they are directly connected with the resistor-ladder, the observability of resistor-ladder in *DAC* is relatively high. Since the TTF of D-flip-flop is relatively low, the three observation points were inserted between the two D-flip-flop groups to improve the observability of digital part. To further improve the overall observability, the clock, a global control signal, is selected as the fourth observation point.

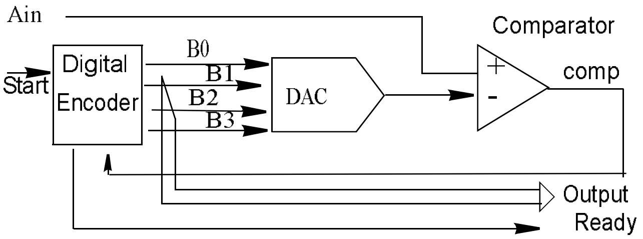


Figure 5: 4-bit successive approximation ADC

As described in these two examples, testability can be increased effectively by the test point insertion procedure presented in this work. These test points can help circuit designers obtain important information to test their circuits.

4.3 Speed of the software

The run time of each testability analysis is determined by the complexity of circuit, the number of components and the number of internal nodes. It is also affected by the circuit matrix setup time and testability calculation time. Each test point selection is the function of number of internal nodes, The following equation estimates run time:

$$T_{run} = T_{set} + (T_{sort} + M \cdot T_{tc})N \qquad (4.3.1)$$

where

T_{run} = run time

T_{set} = circuit matrix setup time

T_{sort} = sort time

T_{tc} = single testability calculation time

M = number circuit nodes

N = number of test points

For large circuit, M is replaced by m_s, the number of given maximum number of nodes each search considers.

Both of the example circuit are processed using Sun work station (Sparc 20). Run times are shown in Table 3.

TABLE 3. Run times of two example circuits

	CPU time	test points	nodes
power supply	717s	4	95
AD converter	303s	4	67

5.0 Conclusions

In this paper, a test point insertion algorithm is developed. A mixed-signal testability analysis procedure was presented based on digital and A/D interface component models. The experiments on two typical mixed-signal circuits indicate the benefits in increasing the testability and the result was compared with designer's selection.

Without using a fault model, our approach can be applied in early design. However, our approach provides no directly connection between testability and fault coverage. In this job, we normalized the testability value. Further work also includes improvement in the speed of the search engine and development of a more hierarchical model to analyze system level testability.

Acknowledgment

Partial financial support for this work was provided by the DARPA/Boeing MiST contract F33615-95-2-5562. The power supply circuit was supplied by Boeing.

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