Bilateral German-Estonian project (2000-2002)

Title: Functional Built-in Self-Test in Digital Systems

Principal investigator: prof. R.Ubar

Partners: FhG Institute of Integrated Circuits, Dresden and University Stuttgart

Abstract: In this project we have investigated the main trends in the field of Functional Built-In Self-Testing (BIST) and we have planned to develop a new method based on the joint competences of the partners of the project. The target of the project is to develop a new method of BIST which exploits the functionality of the system under test itself. Currently we are investigating which extentions are needed to introduce into the Automated Test Pattern Generator (ATPG) to be used in developing this new BIST method. Some new features concerning the defect-orientation in test pattern generation have been investigated in [1,2] with the goal to increase the quality of tests to be generated.

Reports

Functional BIST

(EST 00/001)

Report

Visitor: **Prof. Raimund Ubar (TTU)**
Place: **Fraunhofer Institute Dresden**
Period: **16.12. - 23.12. 2002**

Goals of the visit

The goal of my visit was to draw the conclusions of the results achieved within the project and to discuss about the conception of the R&D activities aimed at a new bilateral WTZ project.

Short description of the work perfrormed during the visit

During my visit at FhG IIS/EAS Dresden we discussed the state-of-the-art of the project and the achieved results. The results can be divided into two parts: 1) to develop a new methodology for designing functional BIST of digital systems in cooperation with University Stuttgart (US), and 2) to integrate the test generation tools of TU Tallinn (TTU) into the environment MOSCITO for providing access to the tools via Internet in cooperation with FhG IIS/EAS Dresden.

1. A general methodology for functional BIST has been developed for sequential circuits (cores in Systems on Chips) by combining two tools: the hierarchical test gnerator developed at TTU and the functional BIST encoding tool developed at US. The methodology was investigated by corresponding experiments carried out first, in Stuttgart and then also in Tallinn with complex digital circuits like DSP cores. Basing on the experimental results it can be stated that the using this methodology the test volume can be reduced about ten times keeping the same fault coverage. A paper on these results is under preparation for the world level International Test Conference.

2. A basis and environment was developed for an Internet-based co-operation in the field of design and test of digital systems. A VLSI design flow can be now combined with an Internet-based hierarchical automated test pattern generation (ATPG). The ATPG can be run at geographically different places under the virtual environment MOSCITO. The interfaces between the integrated tools and also the commercial design tools have been also developed and implemented. During the last project year significant efforts were put to solve the problems of using the tools in MOSCITO in the case of firewall. The functionality of the integrated design and test system has been verified in several co-operative experiments over Internet by partners. The results were presented at the world level events like the conferences DATE in Paris, EUROMICRO in Dortmund, and the workshop on IP-based SOC Design in Grenoble. In total, the results were published during the last 2 years in 7 papers.

During my visit at FhG IIS/EAS Dresden we discussed also about the perspective continuation of the cooperation between FhG IIS/EAS and TU Tallinn.

Based on the recent experience of this cooperation, a joint future work on development of internet based tool-set for teaching and training students of universities and engineers from industry in advanced topics of disaining dependable digital systems, especially systems and networks on chip (SoC and NoC) seems to be extremely attractive and useful for both sides. On one hand, FhG IIS/EAS Dresden has a big experience in developing and using the environment MOSCITO for internet based using of CAD tools and teaching. On the other hand, TTU has a big experience in developing tools for test purposes and using them in research and teaching. From using these experiences in a joint R&D, a high synergistic effect and significant added value can be expected.

TTU has developed during the last years a comprehensive tool-set Turbo Tester for test purposes which has been used successfully both, for industrial purposes (in cooperation with an Estonian company Artec Design Group), and also for teaching purposes in a large scale. The tool-set is currently being used in Sweden for training engineers from SMEs, and it has been used in the research and for teaching purposes at universities in more than 10 countries.

The TT software consists of a set of tools for solving different test related tasks by different methods and algorithms: test pattern generation by deterministic, random and genetic algorithms, test program optimization (test compaction), fault simulation and fault grading for combinational and sequential circuits, multi-valued simulation for detecting hazards and analyzing dynamic behaviour of circuits, testability analysis and fault diagnosis. The representation of the circuit can be given at gate- and macro levels which gives a possibility to investigate the complexity issues of different test algorithms, which will give to the teaching process high didactive impact.

The TT can be used for advanced laboratory work for teaching undergraduate and graduate students at universities, for training experienced engineers in the industry, as well as for life long learning purposes. A lot of different options, available in TT, give students an opportunity to compare different models and methods used in the testing practice. They can investigate by TT the testability of circuits, redesign them if necessary for improving testability, insert self-test BIST structures, analyze the efficiencies and trade-offs of different BIST solutions and learn to make proper engineering decisions in the field of testable design.

Integrating the tools of TT into the MOSCITO environment will give them a new quality. By the use of web-based media we achieve the possibility to use these tools independently of place and time. Individual learning can take place, according to the students‘ own needs. More skilled students can get an extended knowledge and experience in laboratory research. They become able to compare different design, test, and diagnostic methods and will be better prepared for challenges of the new technologies in chip design.

Prof. Raimund Ubar
Dresden, 20. December 2002

Functional BIST
(EST 00/001)

Report No 6

Visitor: **Prof. Raimund Ubar**
Place: **Fraunhofer Institute Dresden**
Period: **24.06. - 29.06. 2001**

Goals of the visit

The goal of this visit was to discuss the main points of the conception of R&D activities for the second year of the project, and to plan a demonstrator of the results achieved.

Short description of the work perfrormed during the visit

During my visit at FhG IIS/EAS Dresden we discussed the strategy for linking the new fault simulation and test generation tools developed at TU Tallinn with the MOSCITO system of EAS with the goal of using these tools via internet.

It was found that there is a need of updating the current status of implementation, especially, to carry out the improvements of the application of MOSCITO in the case of firewall and to generalize the implementation strategy for new components of the design and test software developed or to be developed in the future in Tallinn. The working plan for carrying out the formulated updates and improvements was developed and agreed by partners during the visit. The work will be carried out by Eero Ivask (TU Tallinn) in cooperation with partners of FhG IIS/EAS Dresden during his visit in Dresden in August 2001.

A practical design of a digital controller created at FhG IIS/EAS Dresden was chosen and analyzed to be fault simulated and tested by the tools of TU Tallinn. The corresponding data files were analysed and prepared for the use by the partners of TU Tallinn for carrying out the experimental work via internet. The results of fault simulation and test generation for the controller will serve as a demonstrator of the current project EST 00/001 in the end of the current year.

The results of the work carried out up to now under this project concerning integration of the tools of TU Tallinn with MOSCITO have been published in the following new joint papers:

1. A.Schneider, P.Schneider (FhG IIS/EAS Dresden), E.Gramatova (Institut for Informatics, Bratislava), E.Ivask (TU Tallinn). Internet-basierter Systementwurf mit MOSCITO. Entwurf Integrierter Schaltungen. 10. E.I.S. Workshop, Dresden. April 3-5, 2001.
2. E.Ivask, R.Ubar, J.Raik (TU Tallinn), A.Schneider (FhG IIS/EAS Dresden). Internet-Based Test Generation and Fault Simulation. Design and Diagnostics of Electronic Circuits and Systems. DDECS'2001, Györ, Hungary, April 18-20, 2001.

Prof. Raimund Ubar
Dresden, 28. Juni 2001