Estonian Excellence Centre of Dependable Computing (2003-2007)

Research Team: **Design and Test of Digital Systems (DT)**
Computer Engineering Department

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Research fields: The scientific goals of the DT research group are closely related to the most highly recognized guidelines for design and test solutions of "The MEDEA Design Automation Roadmap". MEDEA (Micro-Electronics Development for European Applications) is a part of the pan-European EUREKA network for cooperative R&D in computer-aided design (CAD) and design automation. The team is involved in the following research fields: design and test of digital systems, self-testing and fault tolerance. The main target of the research is: to develop new efficient methods for modeling, design and test of digital systems to quarantee the efficiency, high quality and fault tolerance of systems in the conditions of continuously increasing complexities. To reach this target the team has competence, and is actively working with the following more specific problems: diagnostic models for digital systems, automatization of test program generation, fault simulation and fault diagnosis in digital systems, physical defect oriented fault analysis, decompositional design and design error diagnosis in digital systems, analysis and partitioning methods for hardware/software codesign, and development of unified representation of systems for control and memory intensive applications.

Most important results of the recent years:

Systems modeling and synthesis. Design/synthesis. Prototype high-level synthesis tool targeting control and memory intensive applications has been developed [1]. The tool makes efficient use of commercial logic synthesis tools thus allowing designers to start with design entry from higher abstraction levels [2]. In the field of emulation, an accelerator for fault simulation based on reconfigurable hardware (FPGAs) was developed with a novel method for fault injection [3-5]. The experimental research demonstrated very high speed in fault simulation of sequential circuits. Compared to software based solutions the speed increased more than 200 times. Experiments also showed that it is beneficial to use emulation for circuits/methods that require large numbers of test vectors, e.g. simulation-based test pattern generation or validation.

Diagnostic modeling. The recent activities of the research group have been related to the fundamental research on mathematical models for diagnostic simulation of digital systems and application research in the field of hierarchical test generation and fault simulation of digital systems. In this field of basic research, the department had a pioneering position in the world with introducing the SSBDDs for the logic level, and generalizing the BDDs for using at higher level abstractions of digital systems [6-17].

The main difference of SSBDDs compared to the traditional BDDs [18] is in the novelty of representing the structure along the functions [19,20]. A uniform multi-level model for digital systems based on DDs as an extension and generalization of the BDDs has been also developed by the group [19,21]. The DD model allowed us to develop efficient methods for simulating digital systems in a very fast way by uniform algorithms at different logic, RTL, ISA or behavioral levels [20-22]. Promising results have been obtained by SSBDDs in delay simulation [23], design error diagnosis [24,25], fault simulation [26,27], and in jointly using SSBDDs and high-level DDs for hierarchical ATPGs [28-30].

Verification and debug. The research group has participated in verification related research in the framework of European 6th FP STREP project VERTIGO (2006-2008) and in the national Development Center programme (2004-2007). The international research partners include universities of Verona, Southampton and Linköping. As a result of these projects, High-level Decision Diagram (HLDD) based modeling for

verification of register-transfer and system level digital systems has been developed [31]. Efficient methods for code coverage analysis and assertion checking [32] using HLDDs have been introduced. In the field of design error diagnosis, a new conception and method was developed, which allows to adopt in a straightforward way the methods and tools of fault diagnosis used in hardware testing for the use in design error diagnosis [33,34]. A new approach for design error diagnosis was developed that does not exploit error models [24,25].

Test generation. A new approach to defect-oriented fault simulation has been developed, based on mapping the physical defects into higher level constraints [35,36]. The first time, a method and tool were created for proving redundancy of physical defects, which allows to evaluate the quality of tests more adequately compared to existing tools [36-39]. The new functional fault model creates a simple conception and basis for hierarchical defect oriented test [35,36].

The results in testing SoC and NoC can be classified as: (1) solving the test application and fault detection problem in GALS structures [40] and (2) design of a reconfigurable embedded test generation solution that supports a trade-off between test speed and test quality and is designed for multi-layer on-chip interconnect structures [41]. Both methods target delay and crosstalk faults. A novel Boundary Scan-like BIST conception for autonomous at-speed testing and diagnosis of interconnects was developed [42-44]. The new paradigm brings a never achieved before high level of universality, scalability, and configuration independence into the at-speed interconnect testing and diagnosis of interconnect.

Most of the previously published NoC test methods are relying on scan-based approaches. In [45,46] the research group proposed an external well scalable test approach that is based on deriving test configurations from functional fault models for the crossbar switch. A new generalized approach to testability calculation was developed [29,47]. Based on the testability guidance, a very fast RT-level ATPG DECIDER [28] has been developed.

Design for testability. In self-test, a close cooperation between TTU and Linköping University, Sweden has given several original results in the area of hybrid BIST. The results have been reported in many high-quality conferences, like DFT, ATS, ETS [48], and in 2 book chapters [55,56]. The new results achieved by the group can be formulated as follows: (1) A novel method for fast cost estimation for variations of test processes with complex structure [48,49]. (2) Based of the fast cost estimation method, very efficient iterative methods were developed for optimizing hybrid sequential and parallel test processes at different constraints [50-53]. A conception and implementation of a hybrid functional BIST was proposed that allows to reduce considerably the hardware cost compared to the traditional BIST methods [54].

Efficient new methods were developed which allow to use BIST for embedded diagnosis purposes [57,58]. The main idea of the methods is based on bisectioning the fault lists instead of bisectioning the test patterns. A considerable increase of speed and resolution of diagnosis was achieved.

Design for dependability. Research results have been published till now mainly in the field of fault injection with purposes of evaluation of the dependability of systems. New hierarchical multi-level techniques for malicious fault list generation for evaluating the fault tolerance is presented [59-61]. The methods are based on using high and low level DDs. Malicious faults are found by top-down technique, keeping the complexity of candidate fault sets at each level as low as possible.

Defended dissertations. Over the last ten years 14 dissertations have been defended in the project's research field (which surpasses the number of people in the research staff): Tammemäe, Dushina, Ellervee, Raik, Brik, Astrova, Jutman, Vaarandi, Fomina, Jervan, Ivask, Lepmets, Listak, Orasson. Six of them was supervised by PI. In the proposed project 15 PhD students will be involved. Two of them (H.Kruus and S.Devadze) have planned to defend the thesis in 2008.

References:

1. P. Ellervee. xTractor: An Academic High-Level Synthesis Tool for Control and Memory Intensive Applications. The 20th NORCHIP Conference, Copenhagen, Denmark, pp.253-258, Nov. 2002.
2. P. Ellervee, E. Ivask, M. Kruus. Improved VHDL Input for High-Level Synthesis Tool xTractor. The 10th Biennial Baltic Electronic Conference (BEC'2006), Tallinn, Estonia, pp.87-90, Oct. 2006.
3. P.Ellervee, J.Raik, V.Tihhomirov, R.Ubar. FPGA Based Fault Emulation of Synchronous Sequential Circuits. Proc. of the 22nd IEEE Norchip Conference, Oslo, November 8-9, 2004, pp.59-62.
4. J.Raik, P.Ellervee, V.Tihhomirov, R.Ubar. Improved Fault Emulation for Synchronous Sequential Circuits. IEEE Proceedings of the 8th Euromicro conference on Digital Systems Design DSD2005. Porto, Aug.30 – Sept. 3, 2005, pp.72-78.
5. P.Ellervee, J.Raik, K.Tammemäe, R.-J.Ubar. FPGA Based Fault Emulation of Synchronous Sequential Circuits. IET Computers & Digital Techniques, Volume 1, Issue 2, pp.70-76, March 2007.

6. R.Ubar. Test Synthesis with Alternative Graphs. IEEE Design and Test of Computers. Spring, 1996, pp.48-59.
7. R.Ubar. Multi-Valued Simulation of Digital Circuits with Structurally Synthesized Binary Decision Diagrams. OPA (Overseas Publishers Assotiation) N.V. Gordon and Breach Publishers, J. of Multiple Valued Logic, Vol.4 pp. 141-157, 1998.
8. R.Ubar, A.Moraviec, J.Raik. Cycle-based Simulation with Decision Diagrams. IEEE Proc. of Design Automation and Test in Europe - DATE. Munich, March 9-12, 1999, pp.454-458.
9. R.Ubar, A.Morawiec, J.Raik. Back-Tracing and Event-Driven Techniques in High-Level Simulation with Decision Diagrams. Proc. of the IEEE ISCAS'2000 Conference, Geneva, May 28-31, 2000, Vol. 1, pp. 208-211.
10. R.Ubar, D.Borrione. Design Error Diagnosis in Digital Circuits without Error Model. In VLSI: Systems on Chip, Kluwer Academic Publishers, 2000, pp.281-292.
11. J.Raik, R.Ubar. Fast Test Pattern Generation for Sequential Circuits Using Decision Diagram Representations. J. of Electronic Testing: Theory and Applications - JETTA. Kluwer Academic Publishers, Vol. 16, No. 3, pp. 213-226, 2000.
12. A.Jutman, R.Ubar, Z.Peng. Algorithms for Speeding-Up Timing Simulation of Digital Circuits. DATE, Munich, March 13-16, 2001, pp.460-465.
13. R.Ubar. Design Error Diagnosis with Resynthesis in Combinational Circuits. J. of Electronic Testing: Theory and Applications - JETTA. Kluwer Academic Publishers, Vol.19, No.1, pp.73-82, 2003.
14. J.Raik, R.Ubar, S.Devadze, A.Jutman. Efficient Single-Pattern Fault Simulation on Structurally Synthesized BDDs. Lecture Notes in Computer Science, Vol. 3463, Springer Verlag, Berlin, Heidelberg, New York 2005, pp. 332-344.
15. J.Raik, T.Nõmmeots, R.Ubar. A New Testability Calculation Method to Guide RTL Test Generation. Journal of Electronic Testing: Theory and Applications – JETTA. Springer Science + Business Media, Inc. 21, pp.73-84, 2005
16. J.Raik, R.Ubar, T.Viilukas. High-Level Decision Diagram based Fault Models for Targeting FSMs. Proceedings of the 9th IEEE Euromicro Conference on Digital Systems Design DSD2006, Cavtat, pp. 353-358, Aug. 31 - Sep. 2, 2006.
17. R.Ubar, S.Devadze, J.Raik, A.Jutman. Ultra-Fast Parallel Fault Analysis on Structural BDDs. European Test Symposion, Freiburg, May 20-23, 2007.
18. R.E.Bryant. Graph-based algorithms for Boolean function manipulation. IEEE Trans. on Computers, Vol.C-35, No8, 1986, pp.667-690.
19. R.Ubar. Test Synthesis with Alternative Graphs. IEEE Design and Test of Computers. Spring, 1996, pp.48-59.
20. R.Ubar. Multi-Valued Simulation of Digital Circuits with Structurally Synthesized Binary Decision Diagrams. OPA (Overseas Publishers Assotiation) N.V. Gordon and Breach Publishers, J. of Multiple Valued Logic, Vol.4 pp. 141-157, 1998.
21. R.Ubar, A.Moraviec, J.Raik. Cycle-based Simulation with Decision Diagrams. IEEE Proc. of Design Automation and Test in Europe - DATE. Munich, March 9-12, 1999, pp.454-458.
22. R.Ubar, A.Morawiec, J.Raik. Back-Tracing and Event-Driven Techniques in High-Level Simulation with Decision Diagrams. Proc. of the IEEE ISCAS'2000 Conference, Geneva, May 28-31, 2000, Vol. 1, pp. 208-211.
23. A.Jutman, R.Ubar, Z.Peng. Algorithms for Speeding-Up Timing Simulation of Digital Circuits. DATE, Munich, March 13-16, 2001, pp.460-465.
24. R.Ubar, D.Borrione. Design Error Diagnosis in Digital Circuits without Error Model. In VLSI: Systems on Chip, Kluwer Academic Publishers, 2000, pp.281-292.
25. R.Ubar. Design Error Diagnosis with Resynthesis in Combinational Circuits. J. of Electronic Testing: Theory and Applications - JETTA. Kluwer Academic Publishers, Vol.19, No.1, pp.73-82, 2003.
26. J.Raik, R.Ubar, S.Devadze, A.Jutman. Efficient Single-Pattern Fault Simulation on Structurally Synthesized BDDs. Lecture Notes in Computer Science, Vol. 3463, Springer Verlag, Berlin, Heidelberg, New York 2005, pp. 332-344.
27. R.Ubar, S.Devadze, J.Raik, A.Jutman. Ultra-Fast Parallel Fault Analysis on Structural BDDs. European Test Symposion, Freiburg, May 20-23, 2007.
28. J.Raik, R.Ubar. Fast Test Pattern Generation for Sequential Circuits Using Decision Diagram Representations. J. of Electronic Testing: Theory and Applications - JETTA. Kluwer Academic Publishers, Vol. 16, No. 3, pp. 213-226, 2000.
29. J.Raik, T.Nõmmeots, R.Ubar. A New Testability Calculation Method to Guide RTL Test Generation. Journal of Electronic Testing: Theory and Applications – JETTA. Springer Science + Business Media, Inc. 21, pp.73-84, 2005

30. J.Raik, R.Ubar, T.Viilukas. High-Level Decision Diagram based Fault Models for Targeting FSMs. Proceedings of the 9th IEEE Euromicro Conference on Digital Systems Design DSD2006, Cavtat, pp. 353-358, Aug. 31 - Sep. 2, 2006.
31. J.Raik, R.Ubar, T.Viilukas, M.Jenihhin. Mixed Hierarchical-Functional Fault Models for Targeting Sequential Cores. Elsevier Journal of Systems Architecture (accepted for publication)
32. M.Jenihhin J.Raik, A.Chepurov, R.Ubar. Assertion Checking with PSL and High-Level Decision Diagrams. Proceedings of the IEEE 8th Workshop on RTL and High Level Testing - WRTLT'07. IEEE Computer Society Press, 2007.
33. R.Ubar, D.Borrione. Single Gate Design Error Diagnosis in Combinational Circuits. Proceedings of the Estonian Acad. of Sci. Engng, 1999, Vol. 5 , No 1, pp.3-21.
34. R.Ubar, A.Jutman. Design Error Localization in Digital Circuits by Stuck-at Fault Test Patterns. IEEE 22nd Int. Conference on Microelectronics, Nis, Yugoslavia, May 14-17 2000, pp.723-726.
35. R.Ubar, W.Kuzmicz, W.Pleskacz, J.Raik. Defect-Oriented Fault Simulation and Test Generation in Digital Circuits. 2nd Int. Symp. on Quality of Electronic Design – ISQED, San Jose, California, March 26-28, 2001, pp.365-371.
36. T.Cibáková, M.Fischerová, E.Gramatová, W.Kuzmicz, W.Pleskacz, J.Raik, R.Ubar. Hierarchical Test Generation for Combinational Circuits with Real Defects Coverage. Pergamon Press. Journal of Microelectronics Reliability, Vol. 42, 2002, pp.1141-1149.
37. J.Raik, R.Ubar, J.Sudbrock, W.Kuzmicz, W.Pleskacz. DOT: New Deterministic Defect-Oriented ATPG Tool. Proc. of 10th IEEE European Test Symposium, May 22-25, 2005, Tallinn, pp.96-101.
38. J.Sudbrock, J.Raik, R.Ubar, W.Kuzmicz, W.Pleskacz. Defect-Oriented Test- and Layout-Generation for Standard-Cell ASIC Designs. Proceedings of the 8th Euromicro conference on Digital Systems Design DSD2005. Porto, Aug.30 – Sept. 3, 2005, pp.79-82.
39. R.Ubar, M.Aarna, H.Kruus, J.Raik. How to Generate High Quality Tests for Digital Systems. IEEE International Semiconductor Conference, CAS'2004, Sinaia, Romania, Oct. 4-6, 2004, pp.459-462.
40. T.Bengtsson, A.Jutman, S.Kumar, R.Ubar. Delay Testing of Asynchronous NOC Interconnects. Proceedings of the 12th International Conference Mixed Design of Integrated Circuits and Systems Kraków, 22-25 June 2005, pp.419-424.
41. T.Bengtsson, A.Jutman, R.Ubar, S.Kumar. A method for crosstalk fault detection in on-chip Buses. IEEE NORCHIP Conference, Oulu, Finland, Nov. 21-22, 2005.
42. A.Jutman. Efficient At-Speed Interconnect BIST and Diagnosis Framework. Informal Digest of Papers of 10th IEEE European Test Symposium (ETS'05), Tallinn, Estonia, May 22-25, 2005, pp. 257-258.
43. A. Jutman, "At-Speed BIST for Board-Level Interconnect", IEEE European Board Test Workshop, Tallinn, Estonia, 25–26 May, 2005.
44. A.Jutman, R.Ubar, J.Raik. New Built-In Self-Test Scheme for SoC Interconnect. Proceedings of the 9th World Multi-Conference on Systemics, Cybernetics and Informatics. July 10-13, 2005, Orlando, Florida, USA, vol.4, pp.19-24.
45. J.Raik, V.Govind, R.Ubar. An External Test Approach for Network-on-a-Chip Switches. Proceedings of the IEEE Asian Test Symposium 2006, Fukuoka, Japan, pp. 437-442, Nov. 2006.
46. J.Raik, R.Ubar, V.Govind. Test Configurations for Diagnosing Faulty Links in NoC Switches. Proc. of the 12th IEEE European Test Symposium, Freiburg, Germany, May 20-24, 2007.
47. J.Raik, V.Govind, R.Ubar. RT-Level Test Point Insertion for Sequential Circuits. Proc. of the IEEE 1st International Workshop on Testability Assessment – IWoTA-2004, Rennes, Nov.2, 2004, pp.34-40.
48. R.Ubar, M.Jenihhin, G.Jervan, Z.Peng. Hybrid BIST Optimization for Core-Based Systems with Test Pattern Broadcasting. 2nd IEEE Int. Workshop on Electronic Design, Test and Applications – DELTA'04, Perth, Australia, 28-30 January 2004, pp.3-8.
49. G.Jervan, Z.Peng, R.Ubar, O.Korelina. An Improved Estimation Methodology for Hybrid BIST Cost Calculation. Proc. of the 22nd IEEE Norchip Conference, Oslo, November 8-9, 2004, pp.297-300.
50. G.Jervan, Z.Peng, T.Shchenova, R.Ubar. A Hybrid BIST Energy Minimization Technique for SoC Testing. IEE Proceedings on Computers & Digital Techniques, July 2006, Vol. 153, Issue 4, pp.208-216.
51. G.Jervan, P.Eles, Z.Peng, R.Ubar, M.Jenihhin. Test Time Minimization for Hybrid BIST of Core-Based Systems. J. of Computer Science and Technology. Nov. 2006, Vol. 21, No. 6, pp. 907-912.
52. R.Ubar, T.Shchenova, G.Jervan, Z.Peng. Energy Minimization for Hybrid BIST in a System-on-Chip Test Environment. Proc. of 10th IEEE European Test Symposium, May 22-25, 2005, Tallinn, pp.2-7.
53. G.Jervan, P.Eles, Z.Peng, R.Ubar, M.Jenihhin. Hybrid BIST Time Minimization for Core-Based Systems with STUMPS Architecture. 18th Int. Symposium on Defect and Fault Tolerance in VLSI Systems. Cambridge, MA, USA, November 3-5, 2003.
54. R.Ubar, N.Mazurova, J.Smahtina, E.Orasson, J.Raik. HyFBIST: Hybrid Functional Built-In Self-Test in Microprogrammed Data-Paths of Digital Systems. Int. Conference MIXDES, Szczecin, June 24-26, 2004, pp.497-502.

55. G.Jervan, R.Ubar, Z.Peng, P.Eles. Test Generation: A Hierarchical Approach. In “System-level Test and Validation of Hardware/Software Systems” by M.Sonza Reorda, Z.Peng, M.Violante. Springer Series in Advanced Microelectronics, Vol.17, 2005, pp. 63-77.
56. G.Jervan, R.Ubar, Z.Peng, P.Eles. An Approach to System Level Design for Testability. In “System-level Test and Validation of Hardware/Software Systems” by M.Sonza Reorda, Z.Peng, M.Violante. Springer Series in Advanced Microelectronics, Vol.17, 2005, pp. 91-118.
57. R.Ubar, S.Kostin, J.Raik, T.Evartson, H.Lensen. Fault Diagnosis in Integrated Circuits with BIST. Proc. of 10th EUROMICRO Conference on Digital System Design - DSD 2007, Lübeck, Germany, August 27 - 31, 2007.
58. R.Ubar, S.Kostin, J.Raik, M.Kruus. Experimental Comparison of Different Diagnosis Algorithms in the BIST Environment. IASTED Conference on Applied Simulation and Modelling - ASM 2007. Palma de Mallorca, August 29-31, 2007.
59. A. Benso, P.Prinetto, M.Rebaudengo, M.Sonza, R.Ubar. A New Approach to Build a Low-Level Malicious Fault List Starting from High-Level Description and Alternative Graphs. Proc. IEEE European Design & Test Conference, Paris, March 17-20, 1997, pp.560-565.
60. A.Benso, P.Prinetto, M.Rebaudengo, M.Sonza Reorda, J.Raik, R.Ubar. Exploiting High-Level Descriptions for Circuits Fault Tolerance Assessments. 1997 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems. Paris, October 20-22, 1997, pp. 212-216.
61. R.Ubar, G.Jervan, J.Raik, M.Jenihhin, P.Ellervee. Dependability Evaluation in Fault-Tolerant Systems with High-Level Decision Diagrams. Proceedings of IWK, Ilmenau, September 10.13, 2007.