APPLICATION FOR AN ESTONIAN- POLISH JOINT RESEARCH PROJECT
UNDER THE AGREEMENT ON SCIENTIFIC COOPERATION
BETWEEN THE POLISH ACADEMY OF SCIENCES AND
THE ESTONIAN ACADEMY OF SCIENCES
2003-2005

ESTONIAN COOPERATING INSTITUTION AND PROJECT LEADER'S NAME (incl. postal address)	**POLISH COOPERATING INSTITUTION AND PROJECT LEADER'S NAME (incl. postal address)**
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Project title (max 10 words): Defect-Oriented Testing of Digital Systems	

Part I. PROJECT DETAILS

1. A summary (in layman's terms) of the project proposal (max 50 words):

The goal of the joint research is to deal with two contradicting problems of testing microelectronics systems: to cope with the increasing complexities of systems based on deep-submicron technologies and to reach high accuracy and reliability of testing.

To solve these problems, a new efficient hierarchical approach will be developed to defect-oriented fault simulation and test generation, based on a new uniform fault model.

2. Scientific aims of the project; details about how the project objectives are to be met; timescales

To reach high accuracy in simulating physical defects in deep-submicron technologies, a new type of fault model and defect-oriented fault simulation methods will be developed.

The complexity of the problem will be handled by raising the abstraction levels from gate to behavioral one by developing a new uniform graph model.

The new fault model allows to transform accurate low level information about defects without loss of information to higher levels with the goal to reduce the complexity of simulation tasks and to achieve high performance in solving test related tasks.

The research efforts of partners are divided in the following way:
- the task of Polish partners is to carry out research in the low layout level close to the physics of defects for obtaining the information, creating all the relationships needed for low-level defect description, and for mapping the defects to the logic level;

- the task of Estonian partners is to develop higher-level models and methods for fault simulation and test generation, using the logic level information about defects generated by Polish partner.

The timing of expected results is planned as follows:

- Development of the new fault model - 2003
- Development of the defect-oriented fault simulator – 2004
- Development of the defect-oriented test generator – 2005

3. Describe the benefit from this collaboration (to both sides)

We see as the outcome of this joint research the following:

- Getting a lot of synergistic effect in the interdisciplinary cooperation by jointly exploiting the experience of Polish partners in low-level electronics (in modeling transistor circuits) and of Estonian partners in higher-level electronics (in modeling gate- and refister-transfer-level systems)
- Getting new scientific results in the border of two disciplines: physics of defects (Poland) and higher-level fault modeling (Estonia)
- Mutually enriching the laboratory environment by changing and jointly developing new tools for defect analysis, fault simulation and test generation
- Mutually improving the teaching level at both universities by introducing new scientific results achieved in this cooperation into the classical courses of electronics design and testing

Part II. ESTONIAN PROJECT LEADER'S PERSONAL DATA

Family name: UBAR	**First name(s):** Raimund
Academic title: Prof., Member of the Estonian Academy of Sciences	**Institution:** Tallinn Technical University
Date of birth: 16.12.1941	**Place of birth:** Tallinn

Present appointment (incl. the starting date):
Professor of Tallinn Technical University

Position(s) held during last 5 years:

Professor of Tallinn Technical University
Visiting professor in Jonköping, Sweden (1 month, 2000)
Visiting professor in Grenoble, France (2 months, 1999)
Visiting professor in Grenoble, France (4 months, 1998)

Academic qualifications (state type and field of degree(s), year of obtaining and the issuing institution)

PhD, 1971, Bauman Technical University of Moscow (Russia)
DSc, 1987, VAK (Russia)

List of main recent publications (up to 6) in refereed journals or monographs during last 5 years

1. A.Jutman, R.Ubar. Design Error Diagnosis in Digital Circuits with Stuck-at Fault Model. *Journal of Microelectronics Reliability. Pergamon Press,* Vol. 40, No 2, 2000, pp.307-320.
2. J.Raik, R.Ubar. Fast Test Pattern Generation for Sequential Circuits Using Decision Diagram Representations. *Journal of Electronic Testing: Theory and Applications. Kluwer Academic Publishers,* Vol. 16, No. 3, pp. 213-226, 2000.
3. R.Ubar. Multi-Valued Simulation of Digital Circuits with Structurally Synthesized Binary Decision Diagrams. *OPA (Overseas Publishers Assotiation) N.V. Gordon and Breach Publishers, Multiple Valued Logic,* Vol.4 pp. 141-157, 1998.

Joint papers with Polish partners (the polish partners names are in bold):

4. T.Cibáková, M.Fischerová, E.Gramatová, **W.Kuzmicz, W.Pleskacz**, J.Raik, R.Ubar. Hierarchical Test Generation for Combinational Circuits with Real Defects Coverage. Pergamon Press. *Journal of Microelectronics Reliability*, Vol. 42, 2002, pp.1141-1149.
5. **W.Kuzmicz, W.Pleskacz**, J.Raik, R.Ubar. Module Level Defect Simulation in Digital Circuits. Proceedings of the Estonian Academy of Sciences, No 7/4, 2001, pp.253-268.
6. M.Blyzniuk, I.Kazymyra, **W.Kuzmicz, W.A.Pleskacz,** J.Raik, R.Ubar. Probabilistic Analysis of CMOS Physical Defects in VLSI Circuits for Test Coverage Improvements. *Journal of Microelectronics Reliability. Pergamon Press.* Vol 41/12, Dec. 2001, pp 2023-2040.

Part II. POLISH PROJECT LEADER'S PERSONAL DATA

Family name: KUZMICZ	**First name(s):** Wieslaw
Academic title: Professor	**Institution:** Warsaw University of Technology
Date of birth: 02.01.1946	**Place of birth:** Warszawa

Present appointment (incl. the starting date):
Professor, Head of the Division of Design Methods in Microelectronics, Institute of Microelectronics and Optoelectronics, Warsaw University of Technology (since 1995)

Position(s) held during last 5 years:

Head of the Division of Circuit and System Design, Institute of Electron Technology, Warsaw, Poland (02.2001 - 01.2002) - on leave from Warsaw University of Technology

Academic qualifications (state type and field of degree(s), year of obtaining and the issuing institution)

M.Sc: in Solid State Electronics, 1970, Warsaw University of Technology
Ph.D: in Microelectronics, 1974, Warsaw University of Technology
D.Sc: in Technical Sciences, 1986, Warsaw University of Technology
Title of professor: 2000

List of main recent publications (up to 6) in refereed journals or monographs during last 5 years

1. Z. Jaworski, I.M.Kudla, W. Kuzmicz and M. Niewczas, Resistive Plate Chamber (RPC) based muon trigger system for the CMS experiment - pattern comparator ASIC, Nuclear Instr. And Meth. In Phys. Res. vol. A (419), str. 707-710, 1998.
2. W.A.Pleskacz, W.Ku_micz, Estimation of the IC layout sensitivity to spot defects, Electron Technology, vol. 32, pp. 182-190, 1999.
3. W.Kuzmicz, Practical application of dynamic "domino" logic in CMOS VLSI integrated circuits, Electron Technology, vol. 32, pp. 215-219, 1999.
4. A. Bardossy, A. Blinowska, Z. Jaworski, W. Kuzmicz, J. Ollitrault, A. Penciolelli, D. Sarna, A. Walkanis, A. Wielgus, A. Wojtasik, Application of Fuzzy Logic to Pacemaker Control, Biocybernetics and Biomedical Engineering, vol. 23, No. 1, pp. 7 - 28, 2003

and joint papers with Estonian partners (see above).

Part IV. Other project participants (both in Poland and Estonia); state names, titles and job status:

Estonian participants:

1. Dr. Jaan Raik, PhD – senior researcher
2. Dr. Marina Brik, PhD – researcher
3. Artur Jutman – PhD student

Polish participants:

1. Dr. Witold Pleskacz, PhD – assistant professor

and Ph.D. students

Part V. Outputs; please state the policy agreed between the groups concerning publication of results and IPR

Publication of results will follow commonly accepted academic standards of ownership and IPR. If there are chances of commercial exploitation of the results (e.g. software developed in the project), an agreement will be negotiated between the partners.

Part VI. EXPECTED VISITS UNDER THE PROJECT		**From Estonia To Poland**	**From Poland To Estonia**
Year 1	Number of weeks Number of visits	4 4	4 4
Year 2	Number of weeks Number of visits	4 4	4 4
Year 3	Number of weeks Number of visits	4 4	4 4

Part VII. Signatures (add date of signing):
Estonian project leader: **Head of Estonian research institution:**
Polish project leader: **Head of Polish research institution:**

TÄIDETUD TAOTLUS ESITADA hiljemalt 10. detsembriks 2002.

Eesti Teaduste Akadeemia välissuhted
Kohtu 6, 10130 TALLINN

Küsimustele vastab Anne Pöitel (tel. 0644 8677, foreign@akadeemia.ee)

NB! It is highly advisanble to submit the application simultaneously to the Polish Academy of Sciences (for further information please contact Mrs. Ewa Wasiak, tel. +48 22 656 6164, e-mail: Ewa.Wasiak@pan.pl).