APPLICATION FOR AN ESTONIAN- POLISH JOINT RESEARCH PROJECT
UNDER THE AGREEMENT ON SCIENTIFIC COOPERATION
BETWEEN THE POLISH ACADEMY OF SCIENCES AND
THE ESTONIAN ACADEMY OF SCIENCES
2007-2009

ESTONIAN COOPERATING INSTITUTION AND PROJECT LEADER'S NAME (incl. postal address)	**POLISH COOPERATING INSTITUTION AND PROJECT LEADER'S NAME (incl. postal address)**
Tallinn University of Technology, Department of Computer Engineering, Raja 15, 12618 Tallinn, Estonia Prof. Raimund Ubar	Warsaw University of Technology Inst. of Microelectronics and Optoelectronics ul. Koszykowa 75, 00-62 Warszawa, Poland Prof. Wieslaw Kuzmicz
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Project title (max 10 words): Analysis and Testing of Physical Defects in Digital Circuits and Systems	

Part I. PROJECT DETAILS

1. A summary (in layman's terms) of the project proposal (max 50 words):

Testing modern microelectronics faces two contradictory problems – accuracy and complexity. The ultimate goal of the project is development of a hierarchical solution that handles the complexity without compromising accuracy. Special benchmarking hardware has to be also developed to evaluate the performance and accuracy of different defect-oriented test generation approaches.

2. Scientific aims of the project; details about how the project objectives are to be met; timescales

New deep submicron technologies bring new challenges to the researchers all over the world. Scaled down feature sizes do not automatically result in scaling the behavior of physical defects. This results in the need for two important research directions:
- analysis and characterization of new types of physical defects;
- fine tuning of existing fault models as well as simulation and test generation algorithms.

These objectives will be met via utilizing the synergistic effect in the interdisciplinary cooperation by jointly exploiting the experience of Polish partners in lower-level modeling (modeling circuits at the transistor and layout level) and of Estonian partners in higher-level modeling (in modeling gate- and register-transfer-level systems).

The research cooperation can be divided into the following main subtasks:
1. Development of a software tool for critical area extraction and probabilistic analysis of defects in interconnects between components in digital circuits. This data will be used by a new layout-driven defect-based TPG.

2. Development of special benchmarking and educational hardware for physical defect study and analysis:
a) Development of new versions of DefSim IC accordingly to new needs and using upcoming CMOS technologies.
b) Analysis of the behavior of CMOS gates and circuits with introduced defects.
c) Development of new teaching lab scenarios for classes in testing and microelectronics.

The timing of expected results is planned as follows:
2007

- development of a software tool for critical area extraction and probabilistic analysis of defects;
- making research towards benchmarking hardware development accordingly to research and educational needs;

2008

- development of a new layout-driven defect-based TPG;
- redesigning DefSim IC based on new ideas and using new CMOS technologies;

2009

- analysis of the behavior of real physical defects implemented in silicon;
- development of new teaching lab scenarios based on new software and DefSim hardware.

3. Describe the benefit from this collaboration (to both sides)

The main benefits for both partners as well as for the whole microelectronics research community could be formulated as follows:

- Getting new scientific results in the border of two disciplines: physics of defects (Poland) and higher-level fault modelling (Estonia);
- Mutually enriching the laboratory environment by changing and jointly developing new tools for defect analysis, fault simulation and test generation;
- Mutually improving the teaching level at both universities by introducing new scientific results achieved in this cooperation into the classical courses of electronics design and testing;
- Serving the testing community by development of publicly available benchmarking hardware for evaluation purposes of different defect-oriented testing approaches.

Part II. ESTONIAN PROJECT LEADER'S PERSONAL DATA

Family name: UBAR	**First name(s):** Raimund
Academic title: Prof., Member of the Estonian Academy of Sciences	**Institution:** Tallinn University of Technology
Date of birth: 16.12.1941	**Place of birth:** Tallinn

Present appointment (incl. the starting date):

Professor of Tallinn University of Technology (since 1987)

Position(s) held during last 5 years:

Professor of Tallinn University of Technology (1987-2002)
Research professor of Tallinn University of Technology (2003-2005)
Visiting professor in Jonköping, Sweden (2 months per year, 2003-2005)
Visiting professor in TU Darmstadt, Germany (2 weeks per year, 2002-2005)
Visiting professor in Jonköping, Sweden (1,5 month, 2001)

Academic qualifications (state type and field of degree(s), year of obtaining and the issuing institution)

PhD, 1971, Bauman Technical University of Moscow (Russia)
DSc, 1987, VAK (Russia)

List of main recent publications (up to 6) in refereed journals or monographs during last 5 years

1. A.Matrosova, A.Pleshkov, R.Ubar. Construction of the Tests of Combinational Circuit Failures by Analyzing the Orthogonal Disjunctive Normal Forms Represented by the Alternative Graphs. J. of Automation and Remote Control. Publisher: Springer Science & Business Media B.V., 66 (2), 2005, pp. 313-327.
2. G.Jervan, R.Ubar, Z.Peng, P.Eles. Chapter 5. Test Generation: A Hierarchical Approach. In "System-level Test and Validation of Hardware/Software Systems" by M.Sonza Reorda, Z.Peng, M.Violante. Springer Series in Advanced Microelectronics, Vol.17, 2005, pp. 63-77.

Joint papers with Polish partners (the Polish partners names are in bold):

3. O. Novak, E. Gramatova, R. Ubar, **W. Pleskacz**, et al.: *"Handbook of Testing Electronic Systems"*, Czech Technical University Publishing House, Prague, September 2005, 395 p., ISBN 80-01-03318-X.
4. T.Cibáková, M.Fischerová, E.Gramatová, **W.Kuzmicz, W.Pleskacz**, J.Raik, R.Ubar. Hierarchical Test Generation for Combinational Circuits with Real Defects Coverage. Pergamon Press. *Journal of Microelectronics Reliability,* Vol. 42, 2002, pp.1141-1149.
5. M.Blyzniuk, I.Kazymyra, **W.Kuzmicz, W.A.Pleskacz,** J.Raik, R.Ubar. Probabilistic Analysis of CMOS Physical Defects in VLSI Circuits for Test Coverage Improvements. *Journal of Microelectronics Reliability. Pergamon Press.* Vol 41/12, Dec. 2001, pp 2023-2040.
6. W.Kuzmicz, W.Pleskacz, **J.Raik, R.Ubar**. Module Level Defect Simulation in Digital Circuits. Proceedings of the Estonian Academy of Sciences, No 7/4, 2001, pp.253-268.

Part II. POLISH PROJECT LEADER'S PERSONAL DATA

Family name: KUZMICZ	**First name(s):** Wieslaw
Academic title: Professor	**Institution:** Warsaw University of Technology
Date of birth: 02.01.1946	**Place of birth:** Warszawa

Present appointment (incl. the starting date):

Professor, Head of the Division of Design Methods in Microelectronics, Institute of Microelectronics and Optoelectronics, Warsaw University of Technology (since 1995)

Position(s) held during last 5 years:

Head of the Division of Circuit and System Design, Institute of Electron Technology, Warsaw, Poland (02.2001 - 01.2002) - on leave from Warsaw University of Technology

Academic qualifications (state type and field of degree(s), year of obtaining and the issuing institution)

M.Sc: in Solid State Electronics, 1970, Warsaw University of Technology
Ph.D: in Microelectronics, 1974, Warsaw University of Technology
D.Sc: in Technical Sciences, 1986, Warsaw University of Technology
Title of professor: 2000

List of main recent publications (up to 6) in refereed journals or monographs during last 5 years

1. A.Bardossy, A. Blinowska, Z. Jaworski, W. Kuzmicz, J. Ollitrault, A. Penciolelli, D. Sarna, A. Walkanis, A. Wielgus, A. Wojtasik, Application of Fuzzy Logic to Pacemaker Control, Biocybernetics and Biomedical Engineering, vol. 23, No. 1, pp. 7 - 28, 2003.
2. A.Wojtasik, Z.Jaworski, W.Kuźmicz, A.Wielgus, A.Wałkanis, D.Sarna: Fuzzy logic controller for rate-adaptive heart pacemaker, Applied Soft Computing, vol. 4. str. 259 – 270, 2004.

Joint papers with Estonian partners (the Estonian partners names are in bold):

3. O. Novak, E. Gramatova, **R. Ubar**, W. Pleskacz, et al.: *"Handbook of Testing Electronic Systems"*, Czech Technical University Publishing House, Prague, September 2005, 395 p., ISBN 80-01-03318-X.
4. T.Cibáková, M.Fischerová, E.Gramatová, W.Kuzmicz**,** W.Pleskacz, **J.Raik**, **R.Ubar**. Hierarchical Test Generation for Combinational Circuits with Real Defects Coverage. Pergamon Press. *Journal of Microelectronics Reliability,* Vol. 42, 2002, pp.1141-1149.
5. M.Blyzniuk, I.Kazymyra, W.Kuzmicz**,** W.A.Pleskacz**, J.Raik**, **R.Ubar**. Probabilistic Analysis of CMOS Physical Defects in VLSI Circuits for Test Coverage Improvements. *Journal of Microelectronics Reliability. Pergamon Press.* Vol 41/12, Dec. 2001, pp 2023-2040.
6. W.Kuzmicz, W.Pleskacz, **J.Raik, R.Ubar**. Module Level Defect Simulation in Digital Circuits. Proceedings of the Estonian Academy of Sciences, No 7/4, 2001, pp.253-268.

Part IV. Other project participants (both in Poland and Estonia); state names, titles and job status:

Estonian participants:

1. Dr. Artur Jutman, PhD – senior researcher
2. Dr. Jaan Raik, PhD – senior researcher

and Ph.D. students

Polish participants:

1. Dr. Grzegorz Janczyk, PhD – assistant professor
2. Dr. Witold Pleskacz, PhD – assistant professor
3. Dr. Andrzej Wielgus, PhD – assistant professor

and Ph.D. students

Part V. Outputs; please state the policy agreed between the groups concerning publication of results and IPR

Publication of results will follow commonly accepted academic standards of ownership and IPR. If there are chances of commercial exploitation of the results (e.g. software developed in the project), an agreement will be negotiated between the partners.

Part VI. EXPECTED VISITS UNDER THE PROJECT		**From Estonia To Poland**	**From Poland To Estonia**
Year 1	Number of weeks	4	4
	Number of visits	4	4
Year 2	Number of weeks	4	4
	Number of visits	4	4
Year 3	Number of weeks	4	4
	Number of visits	4	4

Part VII. Signatures (add date of signing):

Estonian project leader:

Head of Estonian research institution:

Polish project leader:

Head of Polish research institution:

Applicants are asked to **submit a completed and signed form before 2nd May 2006** to:

Eesti Teaduste Akadeemia (välissuhted)
Kohtu 6, 10130 TALLINN

Please address any inquiries you might have to Mrs. Anne Pöitel (tel. +372 644 8677, e-mail: anne.poitel@akadeemia.ee)

NB! It is highly advisable for your **Polish partner to submit the application simultaneously to the Polish Academy of Sciences.** For an application form required and further information, the Hungarian partner is welcome to contact Mr. Janusz Larek, tel. +48 22 656 6280, e-mail: janusz.larek@pan.pl.