REASON (IST-2000-30193)
Final Review Meeting
Workpackage 3

Raimund Ubar
Tallinn University of Technology
raiub@pld.ttu.ee

Final Review Meeting
Sofia, Bulgaria, August 29-30, 2005

- Overview of activities in 2005
- Overview of 2002 - 2005:
  - facts and numbers
  - outcomes vs. expected results
  - self-assessment
  - exploitation plan
- Conclusions

Goals of WP3

WP3 was devoted to

- ***training*** **in design for testability of SoC**
- **developing** ***research skills and creativity***

by

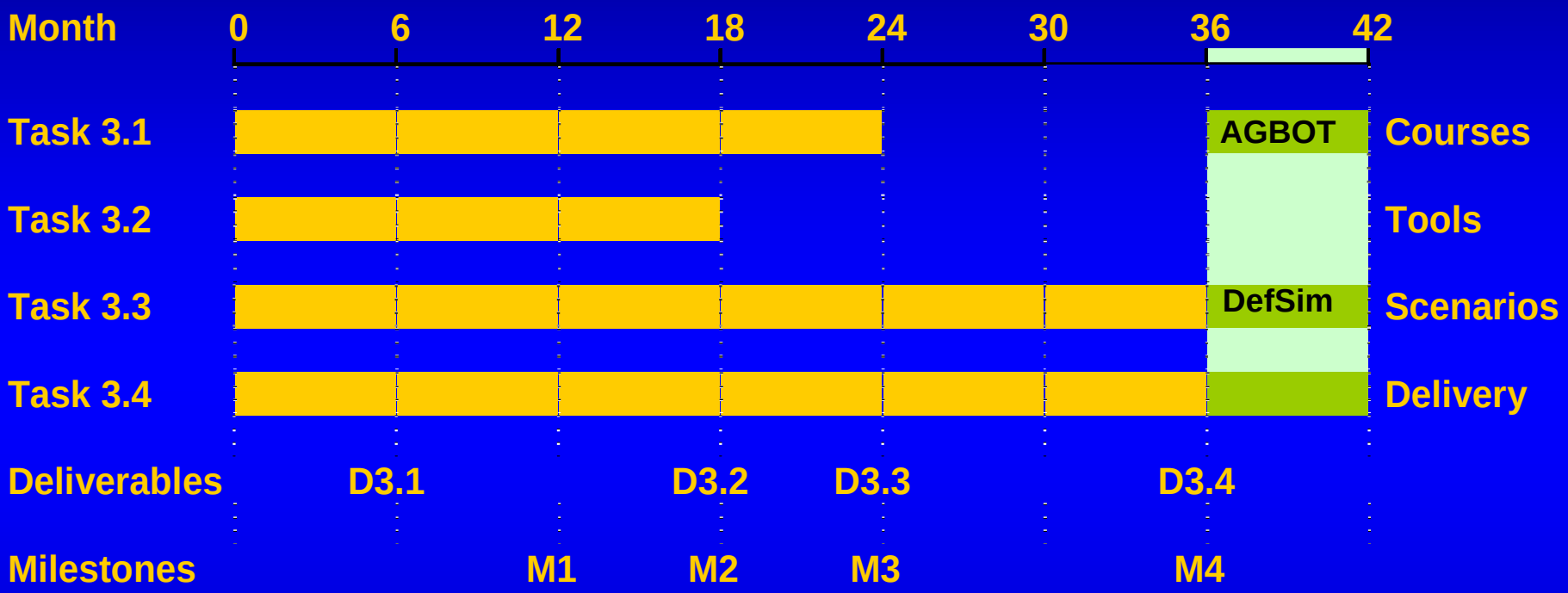
- **development of**
  - ***courses (Task 3.1)***
  - ***tools (Task 3,2)***
  - ***research scenarios (Task 3.3)***
- **dissemination of new methods at**
  - ***tutorials, seminars, workshops (Task 3.4)***

Participants (10 countries)

	Efforts	Task1	Task2	Task3	Task4
• WP leader CR3: TTU (Estonia)	17,4	+	+	+	+
• CO1: WUT (Poland)	0.2	+		+	+
• CR4: VSTU (Russia)	1.1	+	+	+	+
• CR6: FEI STU (Slovakia)	0.2	+		+	+
• CR8: TUI (Germany)	2.0			+	+
• CR13: IISAS (Slovakia)	4.3	+	+	+	+
• CR14: TUS (Bulgaria)	3.8	+			+
• CR15: LPU (Ukraine)			+		
• CR17: TULC (Czech Republik)	4.8	+	+	+	+
• CR18: KTU (Lithuania)	8.0	+	+	+	+
• CR19: BSU (Belarus)	4.4	+	+	+	+

Workpackage 3: activities in 2005

WP3 Timeline



The development activities in T3.1, and T3.3 were mainly related to new initiatives and AGBOT

Events in 2005

- The constant flow of various training actions and other dissemination activities was being kept on the same high level
- 7 tutorials, 1 workshop, 1 project presentation at a National Conference and 3 courses were organized
  - Two 1-day tutorials + 4 embeded short tutorials were co-located with the IEEE 10th European Test Symposium (ETS) (see WP10)
  - The joint REASON WP3/WP7/WP8 workshop was the official fringe event of ETS
- Relation to ETS ensured high attendance of these events by participants outside of the REASON project
- The 1-day tutorials were especially successful with total number of attendees about 60
- 12 travel grants were provided for Eastern attendees of the tutorials

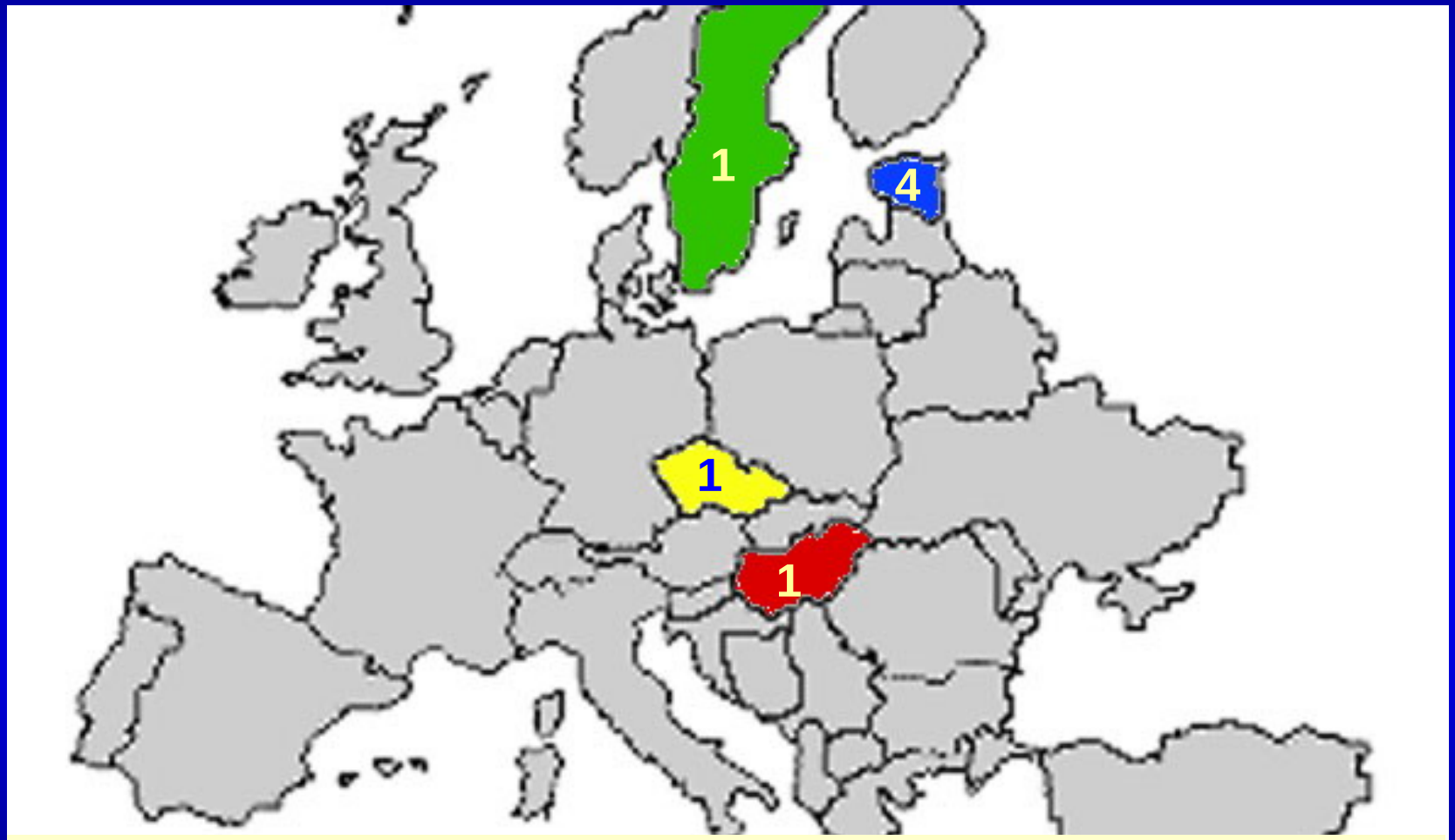
Events in 2005

No	Event code	Event name and organiser	Type	Date	Place	Lang.	No. of part. -------- No. of lect.	Eval.
1	TTU_ JONK05	System Test and Validation TTU	Course, international, open	19.01-13.03. 2005	Jönköping, Sweden	English	2 ------- 20	A: 0 B: 5 C: 4 D: 5 E: 1
2	TTU_ WHY	Why we need deterministic test pattern generation? TTU	tutorial, international, open	13.04. 2005	Sopron, Hungary	English	6 10	A: 0 B: 7 C: 0 D: 0 E: 0
3	TTU_ ETSWS	Testing of Digital Systems TTU	workshop, international, open	21.05. 2005	Tallinn, Estonia	English	9 21	A: 13 B: 3 C: 0 D: 0 E: 0

Events in 2005

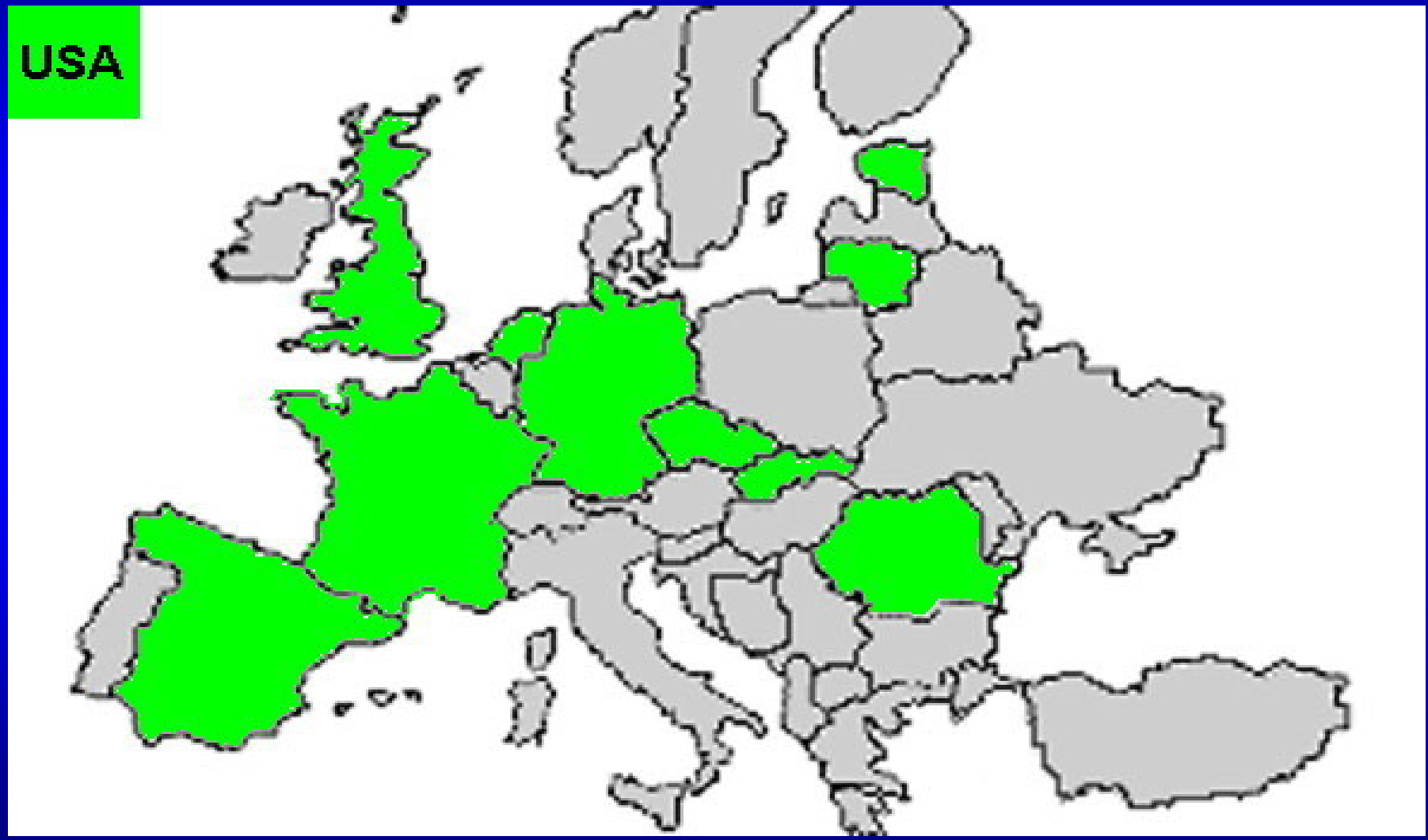
No	Event code	Event name and organiser	Type	Date	Place	Lang.	No. of part. -------- No. of lect.	Eval.
4	TTU_TTEPSOC	System-on-Chip: Embedded Test in Practice TTU,TTEP	tutorial, international, open	22.05. 2005	Tallinn, Estonia	English	1 ------- 40	A: 18 B: 8 C: 0 D: 0
5	TTU_ TTEPAN	Design-for-Test of Analog and Mixed-Signal Integrated Circuits TTU,TTEP	tutorial, international, open	22.05. 2005	Tallinn, Estonia	English	1 ------- 16	A: 2 B: 3 C: 3 D: 0
6	TTU_BORAMB	Formal verification of digital integrated systems TTU, TIMA	course, international, open	02-03.06. 2005	Tallinn, Estonia	English	2 18	A: 5 B: 5 C: 1 D: 0
7	TULC_ TVHDL	HDL based design TULC	Course, national, open	07.06. 2005	Liberec, Czech Rep.	Czech	NA ------- 9	A: 3 B: 6 C: 0 D: 0

Geography of Events in 2005

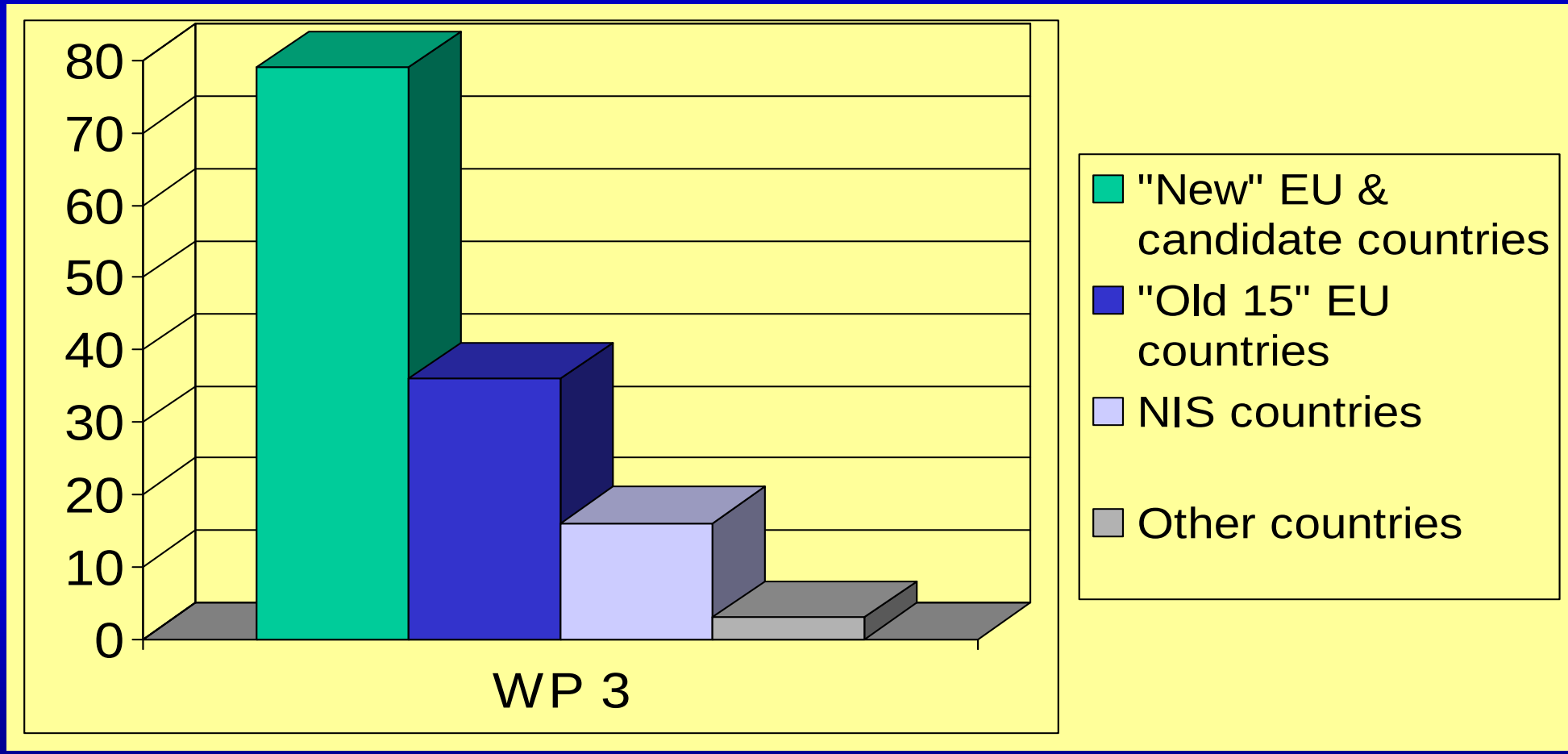


In total: 6 international events out of 7, 3 joint events

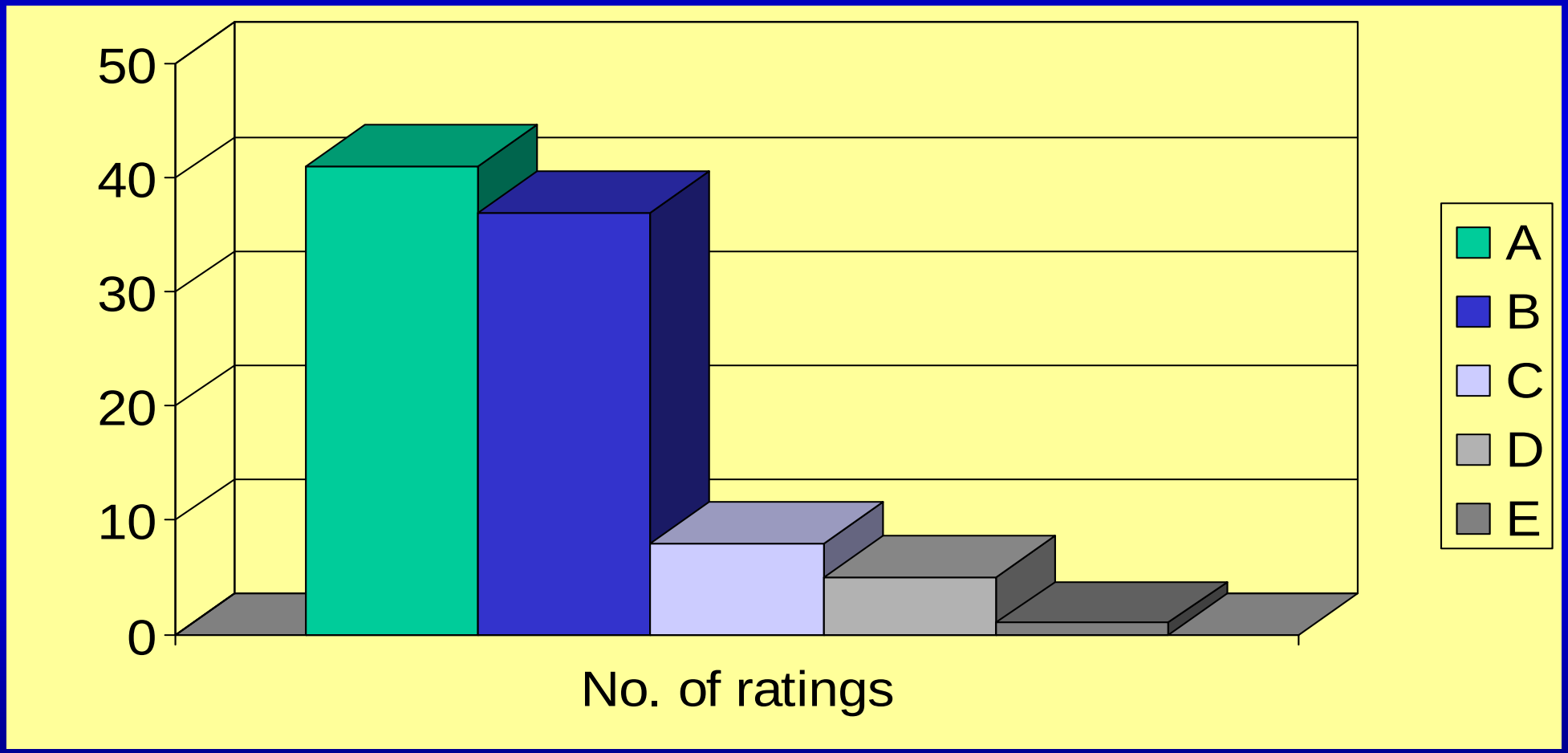
Lecturers 2005



Participants in 2005



Evaluation results in 2005



Other activities in 2005

AGBOT – Handbook of Electronic Testing

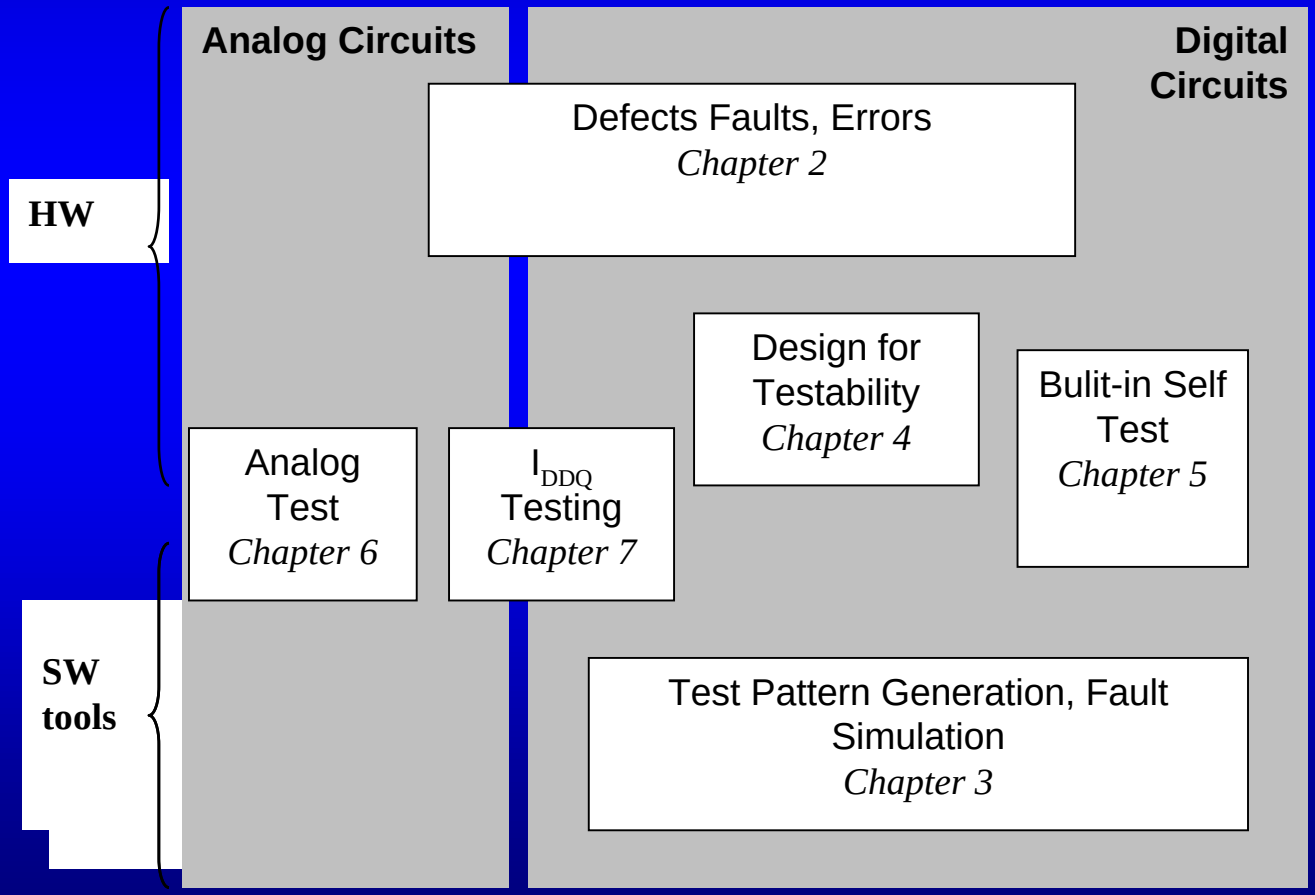
Editors: **O.Novák, E.Gramatová, R.Ubar**

Authors: **(22)**
Czech Republic (9)
Slovakia (5)
Poland (4)
Estonia (3)
Russia (1)

400 pages

Printed: 300 copies by Czech Technical University in Prague

Price: 20 eur



Outcomes: AGBOT

AGBOT – Handbook of Testing

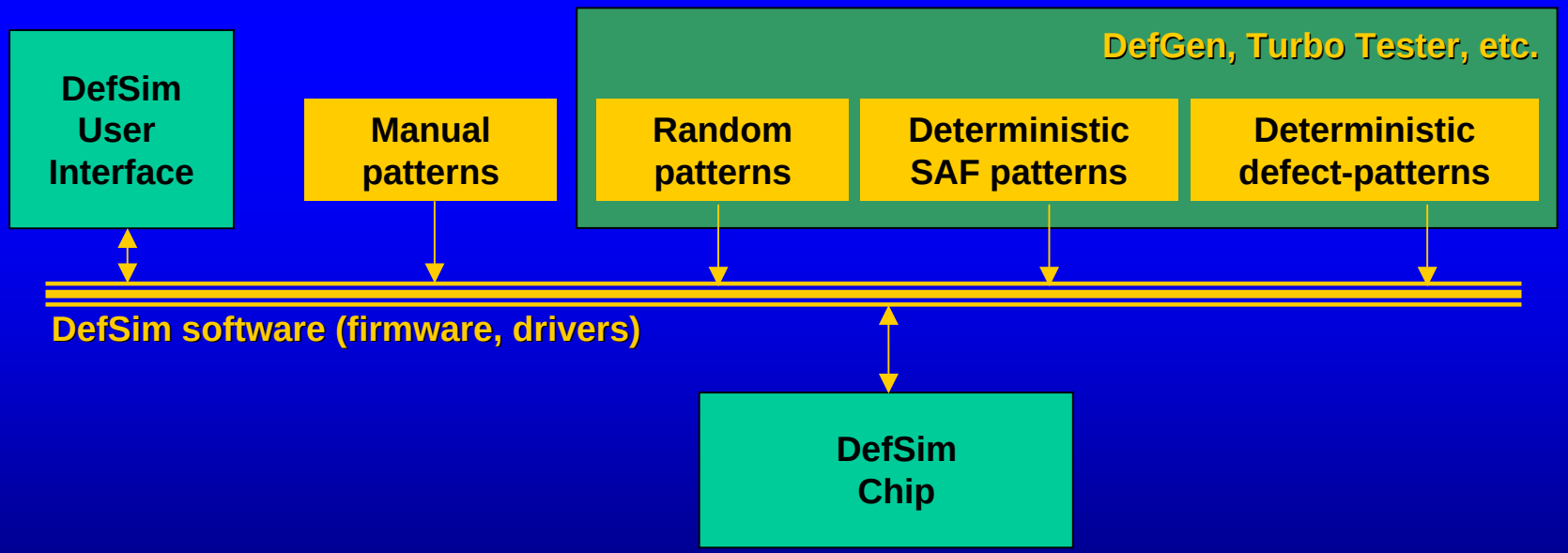
New:

- Broader scope, compared to existing books
- Tools for laboratory research (CD added)
- Theoretical support for Educhips, new lab conception
- A book for teachers
- 5 times cheaper than IEEE/Kluwer books

Appendix 1: Tools developed in REASON
Appendix 2: Philosophy of Mentor test tools

Other activities in 2005

- A lot of activity in WP3 was related to DefSim action of WP9 since the integrated circuit developed in WP9 will serve as a teaching instrument in the courses developed in WP3

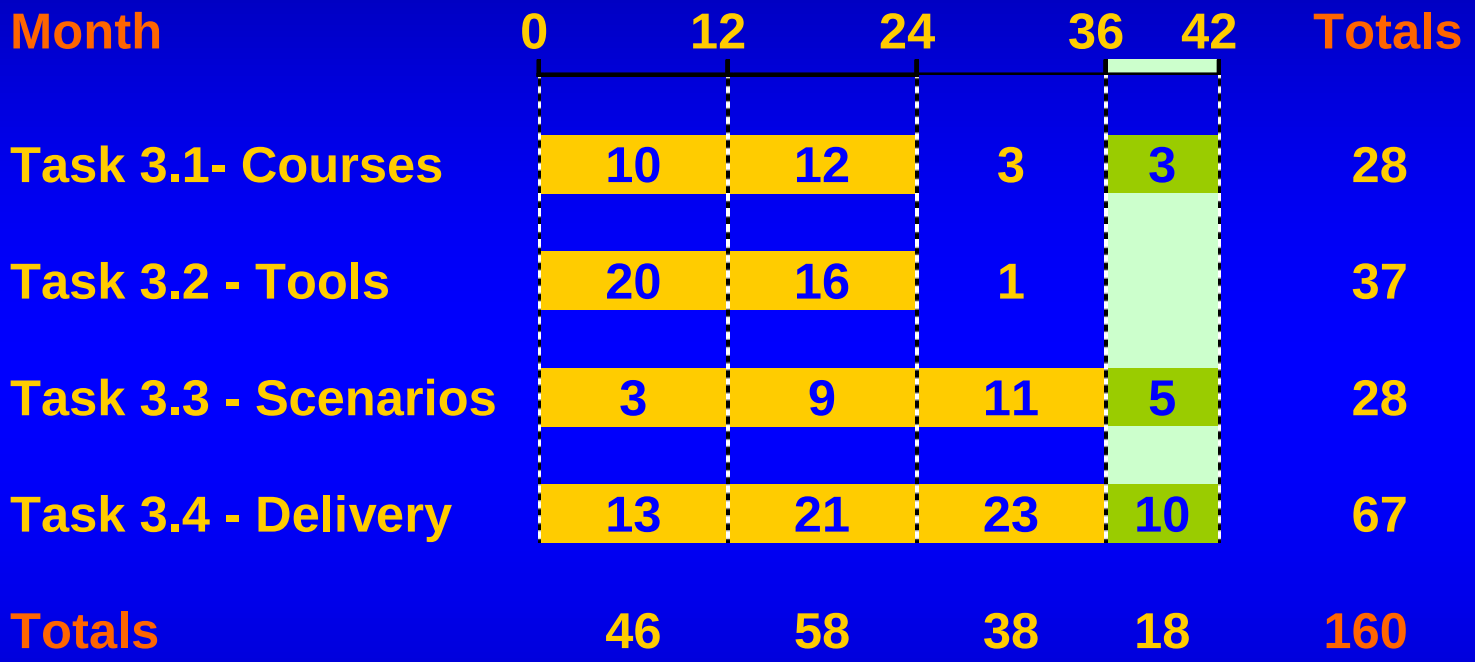


Activities in 2005: Conclusions

- The WP3, in the last stage of the project, was mostly devoted to dissemination (T3.4) of accumulated knowledge and experience in form of tutorials, courses, seminars
- The most of educational tools, teaching materials, and lab scenarios (T3.1, T3.2, T3.3) are completed or undergoing their final testing stage
- All the events scheduled for the year 2005 have been delivered accordingly to the schedule.

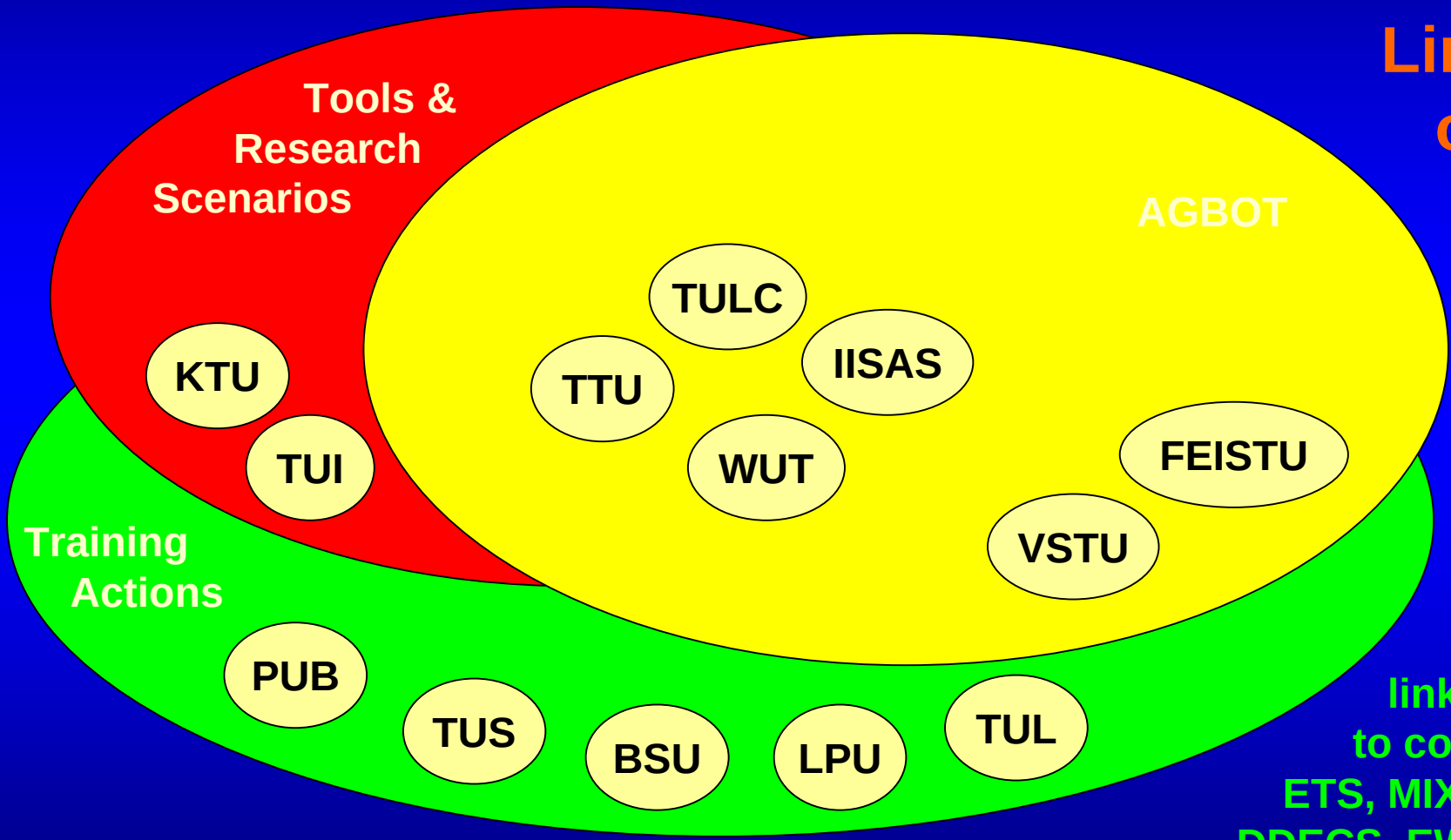
Workpackage 3:
2002 - 2005

WP3 Action Reports



The second year was the most active year since most course materials and tools still had to be completed while dissemination process has already fully started

Cooperation in WP3/WP8/WP9



Links to other WPs:

WP2,6,7
joint tutorials

WP10
linking tutorials to conferences:
ETS, MIXDES, BEC, DDECS, EWDTW

Facts & Numbers

Courses/tools/scenarios:

- Task 1: Number of developed course materials - 28
- Task 2: Number of developed tools - 20
- Task 3: Number of developed lab scenarios - 23

Based on the courses & tools tutorials have been carried out in more than 20 universities in Europe

Dissemination (tutorials, seminars, courses):

- Number of events - 67
- Number of places - 22
- Number of countries - 12

Task 1: Course Development

28 reports

Courses (over 32 h):

- Testing of digital systems (IISAS/FEISTU, TTU)
- Design for testability (TTU, TULC)
- Test and design for dest (BSU, KTU)
- Diagnostics and reliability of digital systems (IISAS/FEISTU)
- Testing of analog circuits (VSTU)

Tutorials (1 day):

- Deterministic test generation and BIST techniques (IISAS)
- Test and diagnosis of analog circuits (VSTU)
- Testing of SoC (TTU)

Joint tutorials (FEISTU, IISAS, KTU, TTU, TULC, VSTU, WUT – 1 day)

- Why we need deterministic test pattern generation?
- Defect oriented testing of ICs and systems
- IC design for testability
- Advanced methods of testing of electronics systems
- Additional hardware for IC testability improvement
- Advanced methods of digital and analog test (Siberian tour)

Task 2: Tool Development

37 reports

- Defect-oriented test generation and fault simulation - IISAS, LPU, TTU (5 tools)
- High-level test generation - KPU, TTU (2 tools)
- Test generation on switch level - BSU
- Boundary Scan and scan-path analysis - TULC (2 tools)
- BIST analysis - TTU, TULC (3 tools)
- Design error diagnosis - TTU (5 tools)
- Test and diagnosis of analog circuits – VSTU
- Test pattern optimization - TULC

20 tools

Task 3: Research Scenarios

Planned in the contract:

- Test Generation and Fault Simulation
- Design for Testability
- Fault Diagnosis
- Built-In Self-Test design and quality analysis

28 reports

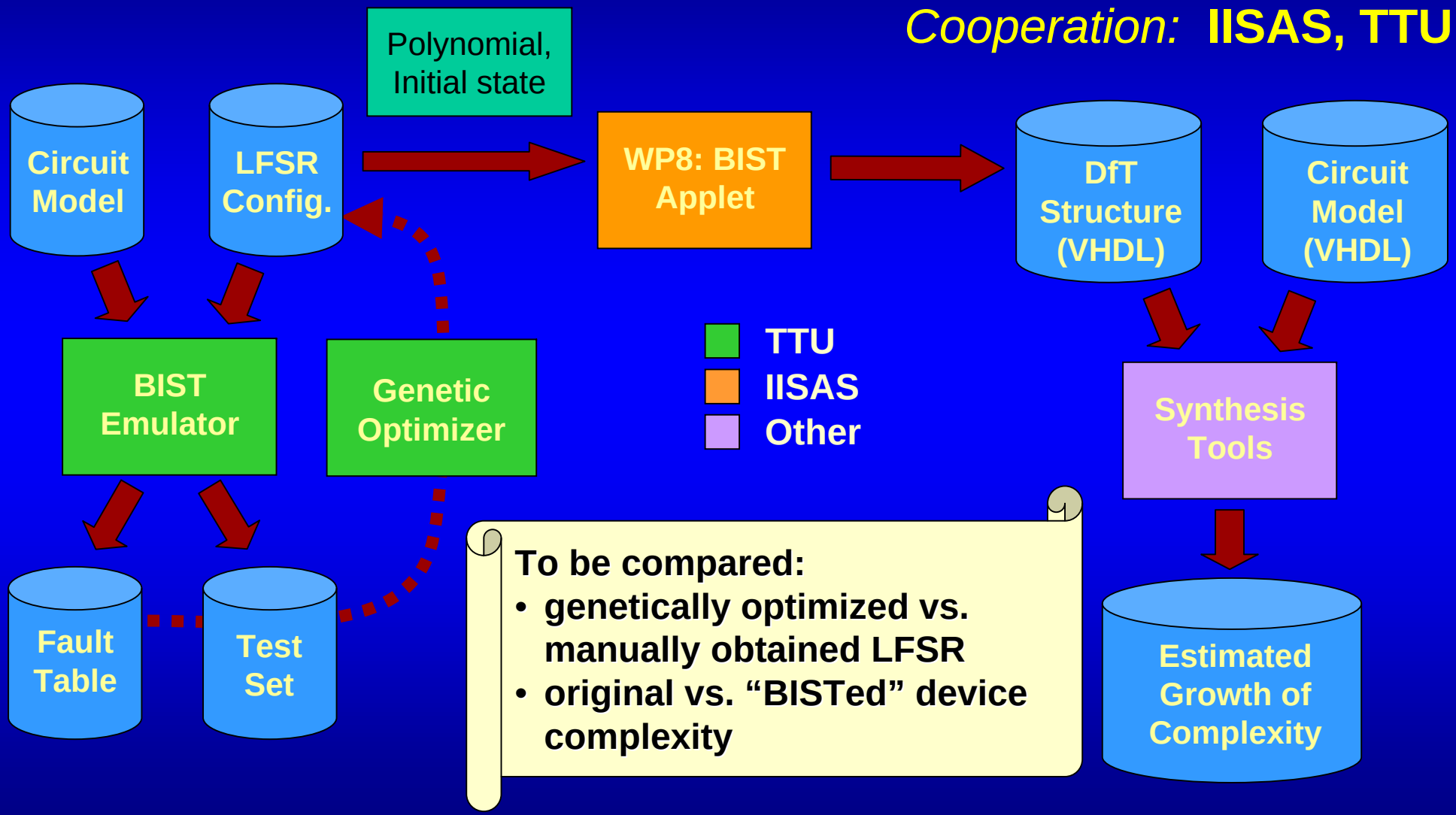
Additionally developed and implemented

- Scenarios for investigation of BIST (5)
  - complexity analysis, architecture analysis, optimization,
  - functional BIST, hybrid BIST
- Applets based scenarios (6)
  - basics of test, RT-level test, Boundary Scan,
  - BIST, MemBIST, Wrapper
- Design for testability research (3)
  - scan-path analysis, study of JTAG
- Advanced test generation topics (4)
  - defect-oriented test, test optimization, genetic algorithms,
  - testing of algorithms
- Educhip-based laboratory works

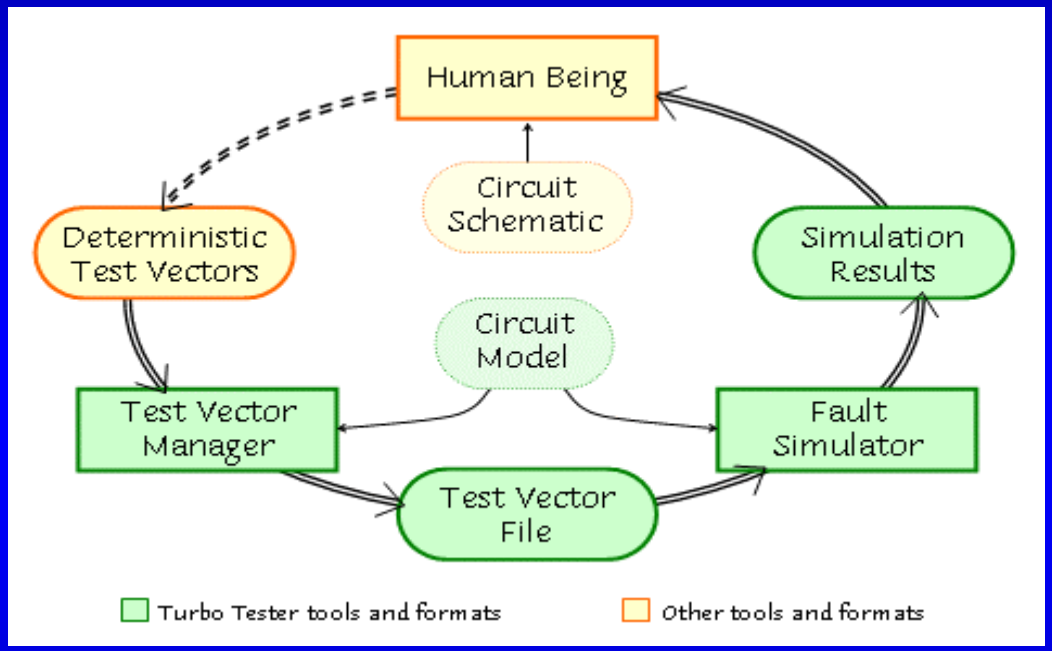
19 scenarios

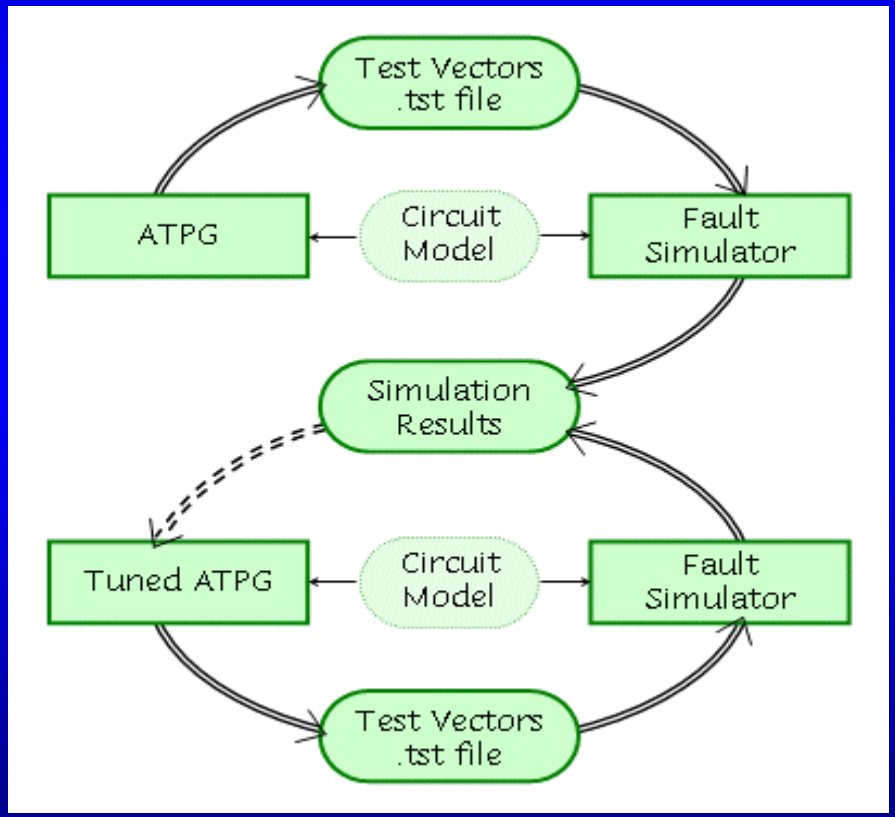
Scenario: BIST Design

Cooperation: **IISAS, TTU**

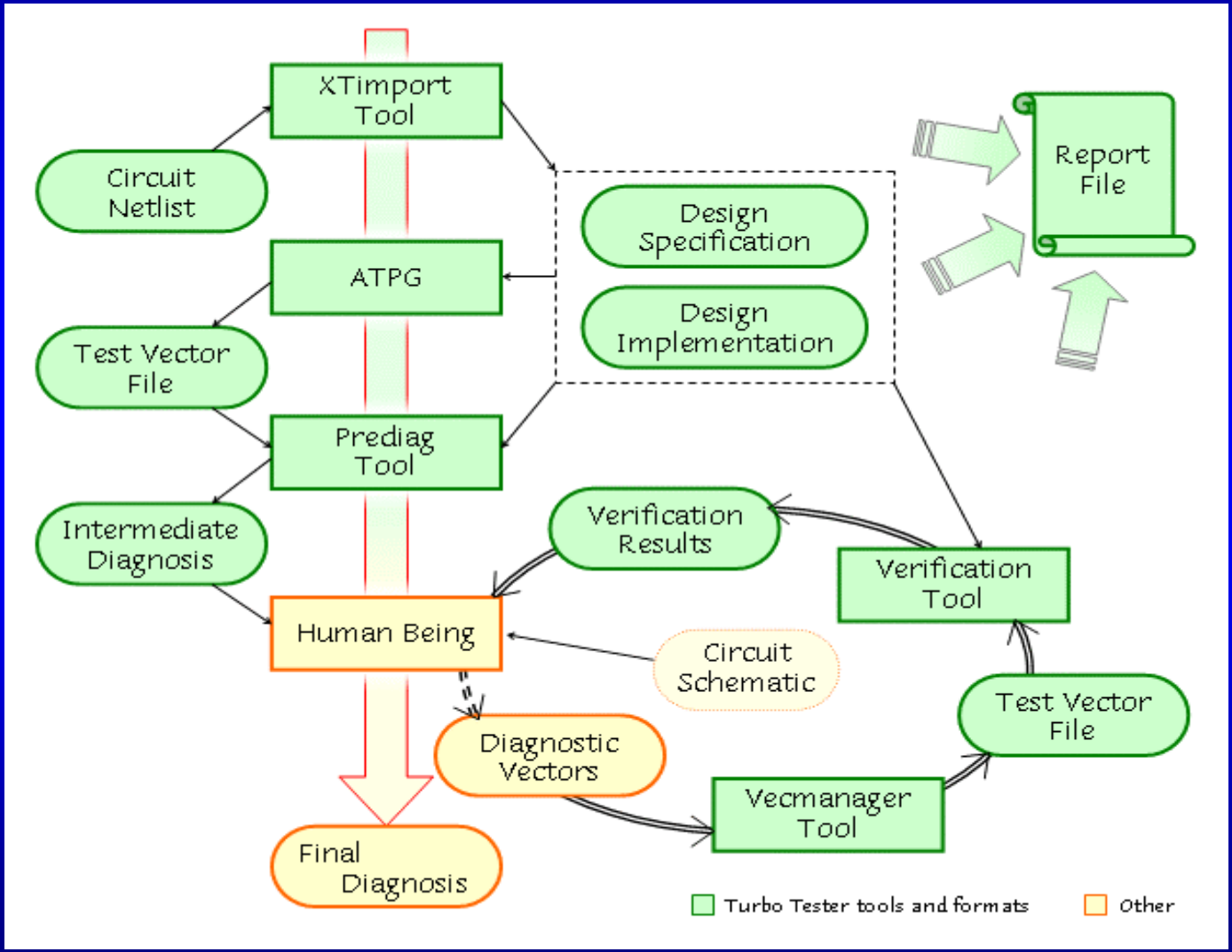


Test Generation Lab

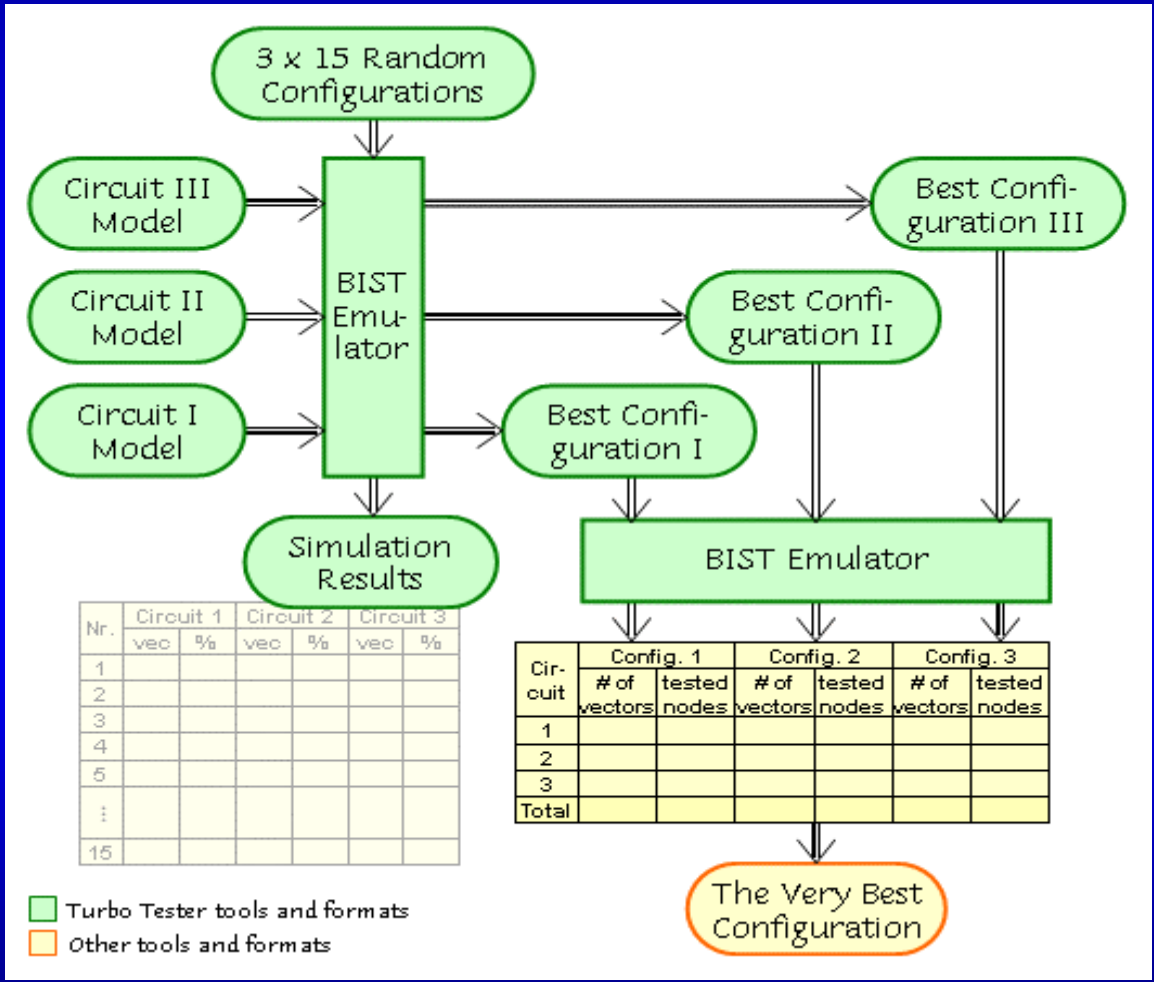




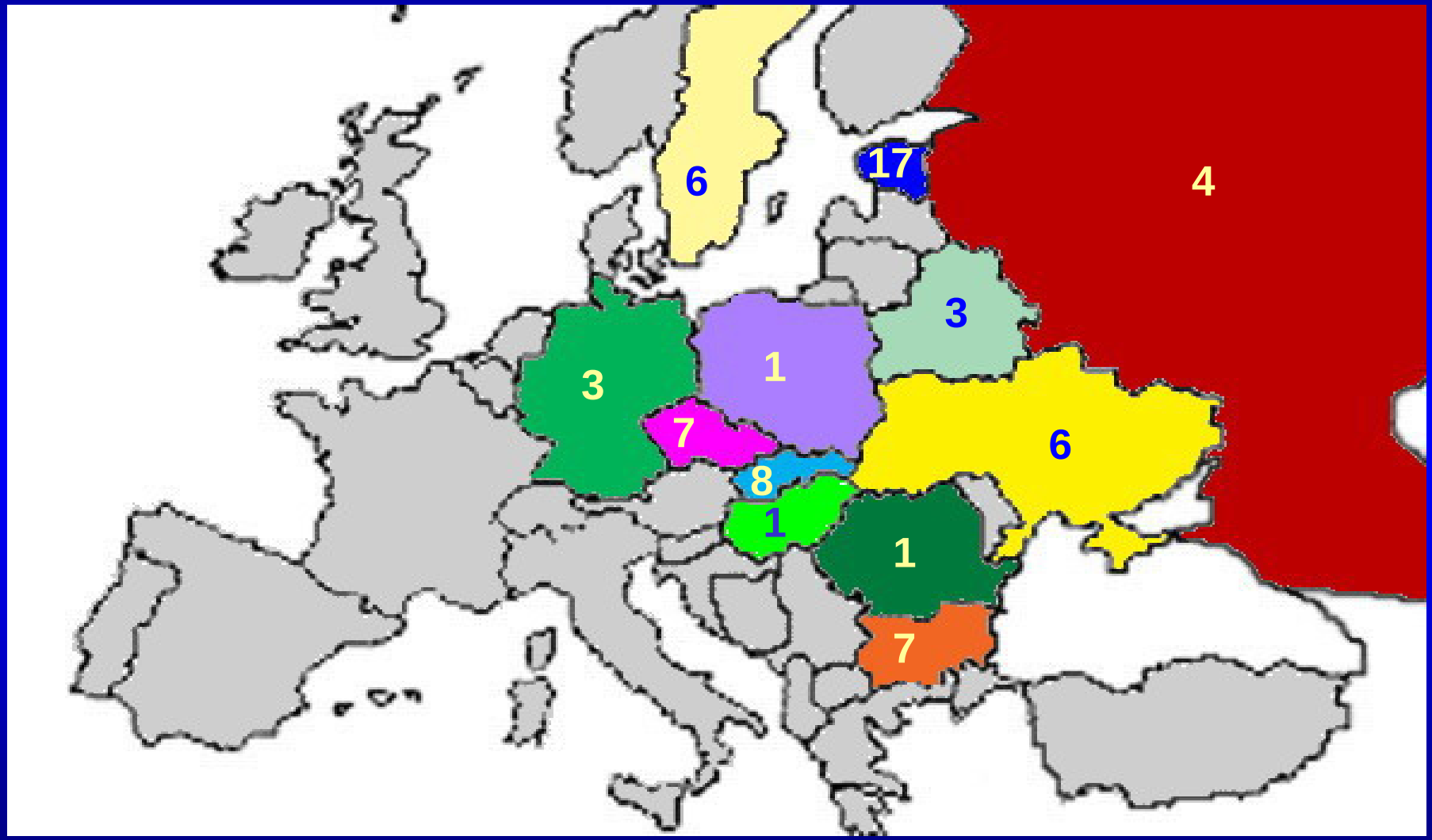
Design Error Diagnosis Lab



BIST Design & Analysis Lab

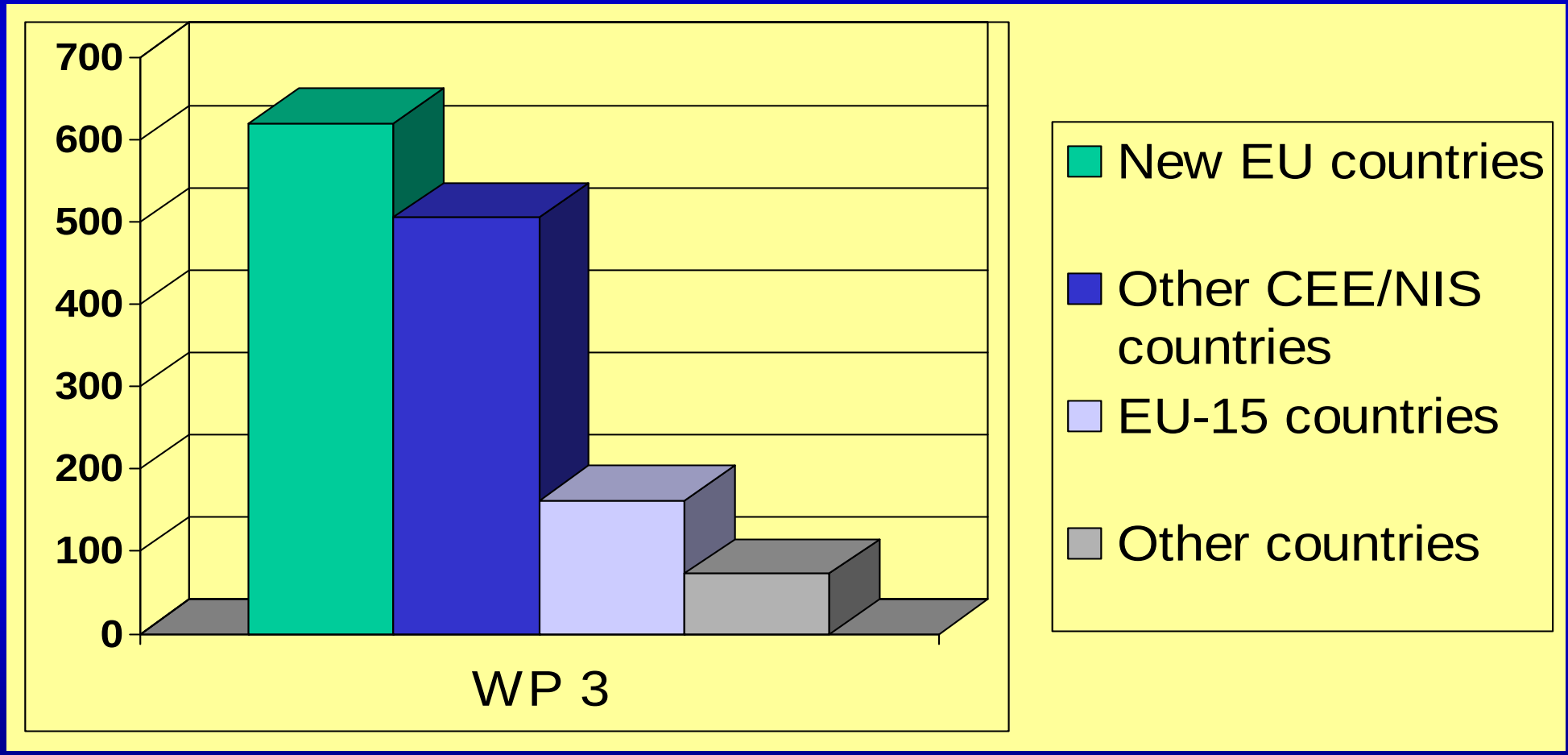


Task 4: Dissemination (all events)



Task 4: Geography of Lecturers

Task4: Participants in All Events



Outcomes: Courses & Tutorials

Bringing expert skills from West to East (>25)

- Y. Zorian, P. Maxwell, D. Floty, W.Wolf - USA
- Ch. Landrault, M.Renovell, A.Jerraya, D.Borionne, P.Amblard, P.Kajfasz, F.Pospiech - France
- M.Glesner, W.Hartenstein, H.-J. Wunderlich, T.Vierhaus - Germany
- H.Tenhunen, B. Magnhagen, S.Kumar, J.Öberg - Sweden
- B. Bennetts – UK
- J. Segura, J.Figueras, J.L. Huertas – Spain
- H.Kerkhoff, L.Jozwiak – Netherland
- M.Austin – Finland
- P.Ienne - Shwitzerland

3 world leading companies (JTAG Technologies, Xilinx and National Instruments) were involved in 4 tutorials and training courses for SMEs

Outcomes: Courses & Tutorials

Knowledge transfer from East to West

Education

- 6 courses (32 h) held in Germany and Sweden
- TT tools is used in >90 institutions in >30 countries all over the World

Industry

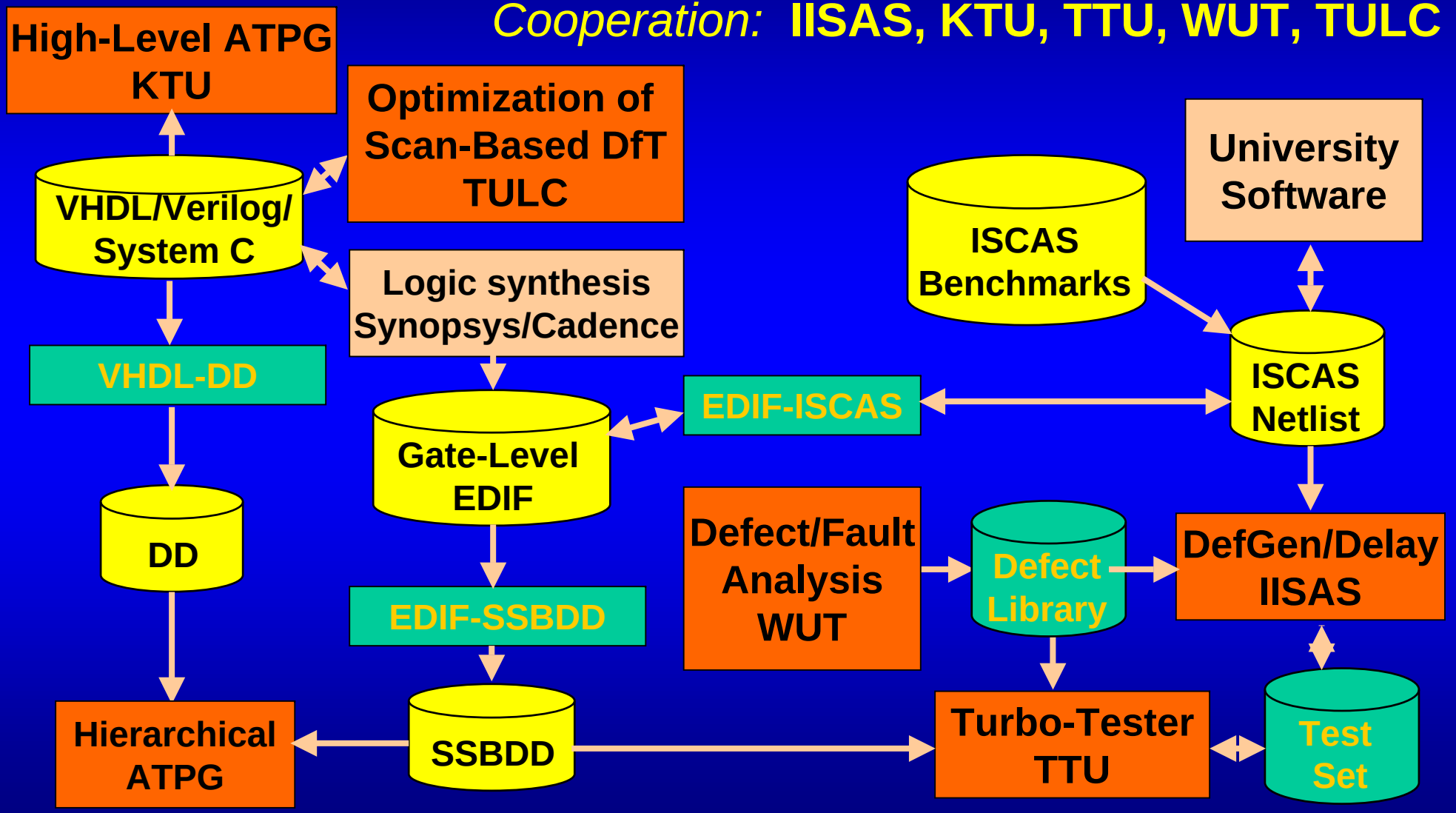
- JTAG Technology is interested to use in his courses for SMEs BS applet
- Contracts are being prepared with Ericsson and Saab for developing BS software tools

Research

- EWD&TW'03'04, ETS'05, EBTW'05: experts from leading centers of REASON-East + Russia, Ukraine, Byelorussia shared their knowledge with western participants
- 15 joint research papers with 8 western researchers

Outcomes: Tool integration

Cooperation: **IISAS, KTU, TTU, WUT, TULC**



Cooperation in Tool Development

Defect-Oriented Test

- TTU: Defect-oriented ATPG and Fault Simulator
- IISAS: Genetic algorithms based defect-oriented ATPG
- LPU/WUT: Cell-oriented Defect/Fault Analysis

BIST

- TTU: BIST quality analysis & hybrid BIST cost optimization
- TULC: Tools for test generation and BIST

High-Level ATPG

- TTU: Hierarchical ATPG
- KTU: Test Generation for testing algorithms

Outcomes: Joint publications

- Number of joint publications – 31
- Book – 1 (AGBOT)
- Journals and chapters of books – 8

  J. of Microelectronics Reliability, JETTA, Design & Test
  J. of Radioelectronics and Informatics, Kluwer, Springer
- Conferences – 22

  DATE, ETS, EDCC, EWME, FIE, LATW, EUROMICRO, MIEL,MIXDES, NORCHIP, EAEEIE, WCETE, BEC a.o.
- Number of REASON co-authors – 39
- Number of co-authors from other countries - 11

Outcomes: New Joint Research

Topics of ongoing joint research (# of joint publ.)

- **Defect-Oriented Test - 10**
  IISAS, TTU, WUT, Darmstadt TU, Politecnico di Torino
- **Built-In Self-Test - 14**
  TTU, Linköping U
- **Engineering Education Technologies - 22**
  Ilmenau TU, TTU, Fraunhofer Institute
- **Network-on-Chip Testing - 2 (2005)**
  TTU, Jönköping University

Outcomes: New Structures

- Two excellent centers in Estonia were founded
  - CDD Research Centre for Dependable Computing
  - ELIKO Development Centre of Mission Critical Embedded Systems (7 SMEs involved)
- ECAD lab in Sofia has changed to a National Competence Center
- Network of educational and research labs in Bulgaria
- A network of SMEs in Lithuania was established
- A new spin-off company Testonica under creation in Estonia

Outcomes vs. goals

Tasks	Goals	Outcomes
T3.1. Full courses	2 (44 h)	8 (>250 h)
Tutorials	5	>10
		AGBOT
T3.2. Tools	10 (SW)	20 (HW/SW)
		Interfaces
		Web-access
T3.3. Scenarios	4	19
T3.4. Events	15	67
Event places	5	22
Joint publications		31

Outcomes vs. goals

Goals: ***new courses, SW tools and lab scenarios to improve teaching in the field of D&T***

Continuous extension of these tasks

2002: from SW tool development to creation of SW/HW based research training environment,

2003: joint textbook AGBOT

2004: web based access to the environment

Continuous joint research, based on the environment with new results - 31 joint publications

2002 - 8
2003 - 3
2004 - 9
2005 - 11

Self-assessment

Positive observations:

Teaching

- Strong impact of the project in improving the level of teaching
- New courses, tools, web-based modules have been created and introduced into teaching
- Our courses and tools have received a broad international recognition, 6 courses (>180 hours in total) have been given in Sweden and Germany
- REASON offered possibilities for students and teachers to participate in summer schools and tutorials with Western lecturers
- New lab environment
  - allows effective teaching and collaboration between partners in research
  - will have a role of an **incubator of new research and pedagogical ideas**

Research

- New joint research directions and cooperations were launched
- Cooperation outside REASON (10 countries)

Self-assessment

Positive observations:

New local structures

- 2 new excellence centres created in Estonia (involving 7 SMEs)
- Establishment of Assotiation of Lecturers, SME leaders, PhD students in Bulgaria
- Establishment of an educational and research labs network in Bulgaria

New international cooperation

- New international projects have been started: MINOS-EURONET THEIERE-DISS
- Cooperation with Eurotraining
- New contracts between universities at international level
- New cooperation contracts with SMEs: e.g. Bulgaria (6), Czech Republic (2), Estonia (7) ...

Self-assessment

The goals or plans not reached:

- **A comprehensive environment consisting of REASON-tools and commercial tools for research and teaching has been developed, but still need further completion**
  - **Some converters between partner tools are missing (VHDL-to-HLDD)**
  - **The user interface to DEFSIM Educhip is in the debugging phase**
- **New goals were set up during the project. Some of these ideas of possible research scenarios have not yet been implemented**
  - **Ideas of the Educhip based defect-oriented testing**
  - **Ideas of the high-level and hierarchical test research**
- **But, there is a big motivation to continue a cooperation between most of the partners to complete these activities**
- **Only a single planned course by TUE (CR 12) was cancelled (due to the changes in staff)**

Self-assessment

Self-critical observations:

- **Sometimes there was a feeling that not all partners devoted equal efforts to launch and carry out joint activities**
- **The man-hours calculated in the project proposal were not adequate to the real time that was spent**
- **Therefore it was not easy to motivate really joint activities**
- **There were two drivers for such a motivation**
  - **joint research interests (perspectives for joint publications)**
  - **enthusiasm and dedication of partners to the task**

Many thanks to all of you who were dedicated!

Exploitation plans

Tools

- A SW/HW based research environment has been created which offers a lot of opportunities to continue cooperation between partners
- The research scenarios will be included into the courses at partners
- The tools will be made available via the framework of EuroTraining "Microsystems University Service" action.

Further development of tools and lab scenarios

- The environment needs further completion and new evaluation
- The development of research scenarios should be continued, especially based on the DEFSIM & TestAccess Educhips
- Some new functions should be implemented e.g. to develop a connection of the TT tools to a PC based scan-path tester (there is a big demand for that in the test community)

AGBOT

- If there is a demand, second edition may be printed
- Translation into the national languages has already begun

Exploitation plan

International cooperation

- There is a big motivation to extend the international cooperation based on this environment beyond the REASON network (Linköping and Jönköping Universities in Sweden, TU Darmstadt, Fraunhofer Institute in Dresden, Politecnico di Torino, KTH etc.)
- Several new European project proposals are under preparation

Cooperation with industry

- SMEs will be involved in the R&D based on the created environment
  - CDD – Research Centre for Dependable Computing
  - ELIKO - Development Centre of Mission Critical Embedded Systems
- A new Spin-Off SME Testonica is under creation
- Further research will be targeted to the activities of I-JTAG and S-JTAG related to Boundary Scan
- A joint work in form of contracts with Ericsson and Saab Testsystems in Sweden is under consideration

Exploitation plans

Continuation of REASON without budget

- DEFSIM labs (in cooperation with WP9) will be introduced into the curricula at TTU this autumn semester with the following expected results:
  - evaluation of the bundle
  - improvement of software
  - improvement of scenarios
- After the evaluation DEFSIM labs will be introduced into the curriculas at IISAS/STU, TULC, WUT a.o. partner places
- A special session at Euromicro Conference in Porto, Sept. 2005
- Preparation of the DEMO-DAY Tutorial of Digital Test with hands-on training for DDECS'06 in Prague to promote the tools developed in REASON

Conclusions

- All the initial targets and goals of WP3 were reached
- REASON allowed to acquire state-of-the-art knowledge, improve teaching and pushing future research in form of a broad international cooperation
- AGBOT – not only a “Great Book”, but also a Great Experience
- Educhip DEFSIM is bringing Teaching of Test from simulated virtual world to the Real Life Level
- REASON had an impact (knowledge transfer) in 2 directions:
  West-to-East, East-to-West
- Working connections (cooperation, contracts, joint centres) were created to industry
- We learned all a lot from the excellent management of the project run by prof. Wieslaw Kuzmicz

A lot of thanks to the Project Coordinator and to the whole REASON Project Team