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1. General Developments

Following the ATSEC review in March 1995, work in the ATSEC project has focuses on cooperative efforts in key areas that might be of specific importance for the commercialisation or at least the further industrial use of ATSEC results.
In particular, the differing approaches towards automatic test generation for large sequential circuits by Politecnico di Torino and by GMD have been combined for an added value. Additionally, the cooperation between GMD and U. Twente towards delay-fault test for sequential circuits continued. The cooperation between GMD and U. Duisburg in the area of constraint-driven and hierarchical ATPG also showed some new results. The problem of hierarchical RT-level test generation was also tackled by TU Tallinn following a previously developed approach based on alternative graphs.

2. "Classical" ATPG Tools

In the first two years of the project ATSEC had focuses on a somewhat "refined" way of test generation that covers non-conventional circuit structures and offers sophisticated fault models beyond "stuck-at".
Most of the work done in this are was published between 1993 and 1995. Also the concept of employing SEMILET, an advanced structural ATPG-tool as a "baseline" tool for extension towards more sophisticated approaches, became quite successful. Today SEMILET is not only the base of U. Twente's delay fault ATPG for sequential circuits (published EDAC-ETC 95), but has also documented its usefulness in tools for combinational and sequential logic optimisation.
ATPG-based optimisation of sequential circuits is, to our best knowledge, truly novel and has raised quite a lot of interest.

These tools were developed jointly by GMD and University of California, Santa Barbara (Prof. Tim Cheng), with emphasis at GMD. They were presented at Asian DAC conference in Sept. 1995. A further paper showing the applicability of "classical" ATPG to gate-level verification was submitted for publication. In this area, Santa Barbara is the topic leader.
Being part of the present surge in "test synthesis", the optimisation tools have raised some industrial interest (particularly Fujitsu, USA).

For the "classical" structure-oriented ATPG tools, despite the successful expansion to more advanced fault models, the general problem still left is a limited handling

capability of large sequential circuits beyond about 10 000 gates, where SEMILET showed unacceptable run times (like all other classical ATPG tools including HITEC).

Since about 1994, ATSEC partners (Pt. di Torino, GMD, U. Duisburg) have tried to solve this problem using two approaches:
- Extremely fast and efficient methods working at the gate level (for stuck-at faults)
- Hierarchical approaches and mixed functional / behavioral methods

3. Advanced "flat" ATPG Methods

Politecnico di Torino has worked on symbolic- and on fault-simulation based ATPG tools for a number of years.
Starting in 1994, GMD and Politecnico di Torino combined SYMBAT, a symbolic ATPG tool, and SEMILET. First results that documented the success for medium-large circuits, were published at the VLSI Test Conference in April 1995. Since then the method has been improved and refined. Concerning large complexities, this is not yet a real break-through.
Since 1994, Pt. di Torino has developed fault-simulation based ATPG tools that use genetic algorithms for optimisation of test sequences.
As demonstrated by Pt. di Torino and other authors, such an approach will handle even the most complex circuits, but will not easily reach the high fault coverage figures that are common to "classical" tools.
Furthermore, fault-simulation based ATPG will not identify redundant and untestable circuit structures.
For this reason, Pt. di Torino and GMD also tried a coupling of Torino`s GATTO with SEMILET. The trick used was to have SEMILET generate patterns that have to be applied at the fault location, but not propagated to primary outputs of the circuits. Such patterns were intended to be used for overcurrent (IDDQ) test, a feature that SEMILET has anyhow.
First, due to the simpler generation process, SEMILET generates fewer patterns in a shorter time and can therefore handle larger circuits. Also circuit analysis for redundancy identification is employed.
Second, these "simple" patterns seem to serve reasonably as "seeds" for the genetic ATPG process in GATTO. The "guided seeds" result in both shorter times and better fault coverage figures from GATTO.

In the fall of 1995, Pt. di Torino and GMD are going for a 3-step approach:
1. structural ATPG for circuit analysis and generation of "seeds"
2. genetic ATPG for the "easy" faults
3. final deterministic ATPG for remaining "hard" faults.

First results compare quite favourably with anything published in the area recently yet (e. g. coupling of HITEC and a genetic ATPG done at U. Illinois by Rudnick and Patel) and will be published in 1996.

New in the fall of 1995, a parallel and distributed version of SEMILET is also running on workstation networks with about a linear gain in performance. Pt. di Torino has

also developed a massive parallel version of GATTO, which is currently using the Connection Machine installed at GMD and will be migrated to an IBM SP-2 in the fall of 1995. (Note: the cooperation in massive parallel computing is done in an advanced EU-project partly based on ATSEC). Possibly after the end of ATSEC, GMD and Pt. di Torino will continue their cooperation in sequential ATPG on parallel machines. It should be remarked that genetic algorithms are much easier to parallelise than any hierarchical ATPG scheme we know by now, resulting in a potential edge in performance.

4. Hierarchical ATPG

In this area, first experience was gained by GMD in 1992/93 with the coupling of switch-level / gate-level ATPG tools for combinational circuits (MILEF). Both extraction of constraints at the higher level and communication of patterns with "rejects" between levels (gate- versus switch-) were implemented successfully.

However, already the experience gained there indicated that the constraint extraction is not simple and most likely incomplete, making "rejects" in hierarchical ATPG still necessary.

As a first step towards sequential circuits, the University of Duisburg has implemented a constraint-control mechanism for a structural ATPG tool (DUST). Remarkable gains in run time and fault coverage could be documented for a few circuit examples. Thereby "constraints", concerning e. g. the setting of clock-and control lines, were defined and set manually.
With this experience it was clear that a "conventional" structural ATPG tool was a candidate for guidance by constraints. (Note that other authors only used a fault-simulation based ATPG approach guided by constraints).
Since 1993, researchers at GMD and in Duisburg have then investigated on the "extraction" and formalisation of constraints at appropriate circuit levels. A first experience was that published approaches (like Abraham et. al. in 1994) are over-simplified and would not work on real circuits. Simply the extraction of a close-to complete set of constraints from a circuit description is extremely complex, unless the "right" type of description is available. Some publications in the field simply work on over-optimistic assumptions: One often-found assumption, for example, is that a faulty sequential subcircuit circuit behaves as "good", if it is traversed again in the ATPG-process via a feedback loop.

The possible solution of the problem included more efforts and tools than expected in 1994.
Automatic extraction of constraints from a structural (gate- or RT-level-) description is close to impossible. Therefore a hierarchical circuit description, which will be based on hierarchical and structural descriptions for modules, is a must. VHDL is a prime candidate.

The work done so far by U . Duisburg and GMD covers the following aspects:
GMD has developed an extraction of constraints from behavioral descriptions in the CASTLE HW / SW co-design system. Results still have to be validated.

This is to be seen as a synthesis link.

Duisburg has so-far concentrated on an efficient use of an existing behavioral APTG tool (FUNTESTIC) and modified it for coupling with a structural ATPG tool, which will be either MILEF (for combinational logic blocks) or SEMILET (for sequential logic). First experiments also use Duisburg`s structural ATPG tool DUST.

In general, a circuit partitioning where "local" structural ATPG is limited to combinational modules and sequential structures are employed only for traversal of patterns is considered quite favourable.
Then the behavioral ATPG, after being triggered to "transport" a pattern to or from the input / output of a "faulty" block, for which a structural pattern is generated, will find a reasonable functional state which is appropriate.
In case the block under test is sequential in itself and has only internal feedbacks, a sequential ATPG like SEMILET can be employed.
The problem case is when the assumed "faulty" block under test has external feedback loops that run through other blocks. Then, for the traversal through the "faulty" block, it would need a functional description under the fault condition, which is not easily available.
Then a check is necessary, if the fault affects the functionality needed for the traversal. If no, the functional model can be used. If yes, a path-oriented structural propagation is necessary.

It is expected that the cooperation between Duisburg and GMD will produce a hierarchical behavioral / functional ATPG facility until the end of the project for the favourable cases shown above.

Note that for any hierarchical and mixed-level work there are no standard benchmark circuits available. Most of the examples had to be synthesised using e. g. SYNOPSYS tools.

5. Delay fault test generation and -diagnosis

In this working area, a transfer of results and tools between TU Twente and LIRMM at Montpellier took place, providing Montpellier with the required delay-fault ATPG tool.
TU Twente, often in close cooperation with GMD, has continuously improved the sequential ATPG tool for delay faults (TDGEN / SEMILET).
By this time, a path-oriented delay fault test generator has been built.

At Montpellier, after conclusion of the basic studies, delay fault diagnosis tools for combinational and sequential circuits were implemented. Work during the latest months included refinement, tuning and experimental use in combination with other ATSEC tools.

6. Testable Design: Built-in Current Monitoring

During the reporting period, major activities for the development of an external current monitor continued at KIHWV in cooperation with an industrial partner. A second generation of current monitors is under construction. On the other hand, Slovak TU has continued the development of a different built-in current monitor. The work on GMD's threshold-programmable built-in current monitor was resumed, layout was finished in May 1995.

KIHWV and Slovak TU have also compared ATSEC tools with other available ATPG tools.
As some of the most advanced commercial tools, e. g. HITEC, were not available in the ATSEC community, comparisons have been limited so far.

7. Other Activities

GMD has established contacts with European and US-based companies that might be interested in either the use or the marketing of ATSEC results.
A remarkable interest was found in the combination of test generation and circuit optimisation tools.
GMD has also started the preparations for a final ATSEC workshop on Sept. 28th / 29th to be held at St. Augustin, Germany.

A documentation describing the functionality of ATSEC tools and their possible application in IC and systems design has been written, published and distributed by GMD to industries.
This volume has already been used for the information of potential industrial users. It is also implemented for access via the World Wide Webb (WWW).

In a new project that includes industrial partners, Politecnico di Torino and GMD have started to develop adapted test generation tools for massive parallel computer systems, based on ATSEC results.

8. Remaining Work

GMD is currently preparing for the ARCHIMEDES-ATSEC Workshop on Sept. 28th / 29th at GMD.

During the remaining time of the project (2 months at present), the main activities will be:

- Coupling of behavioral and structural ATPG in hierarchical circuits
- Optimised coupling of GATTO and SEMILET
- Some performance comparisons with commercial ATPG tools.

The chances to have relatively stable ATPG tools from ATSEC that outperform any commercial tool by far in performance and, alternatively, tools that have capabilities for advanced fault models not available commercially, by the end of the project, are very good.