EVikings II

Establishment of the Virtual Centre of Excellence for IST RTD in Estonia

IST-2001-37592

WP 4
Supporting RTD in Digital Systems

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Overview

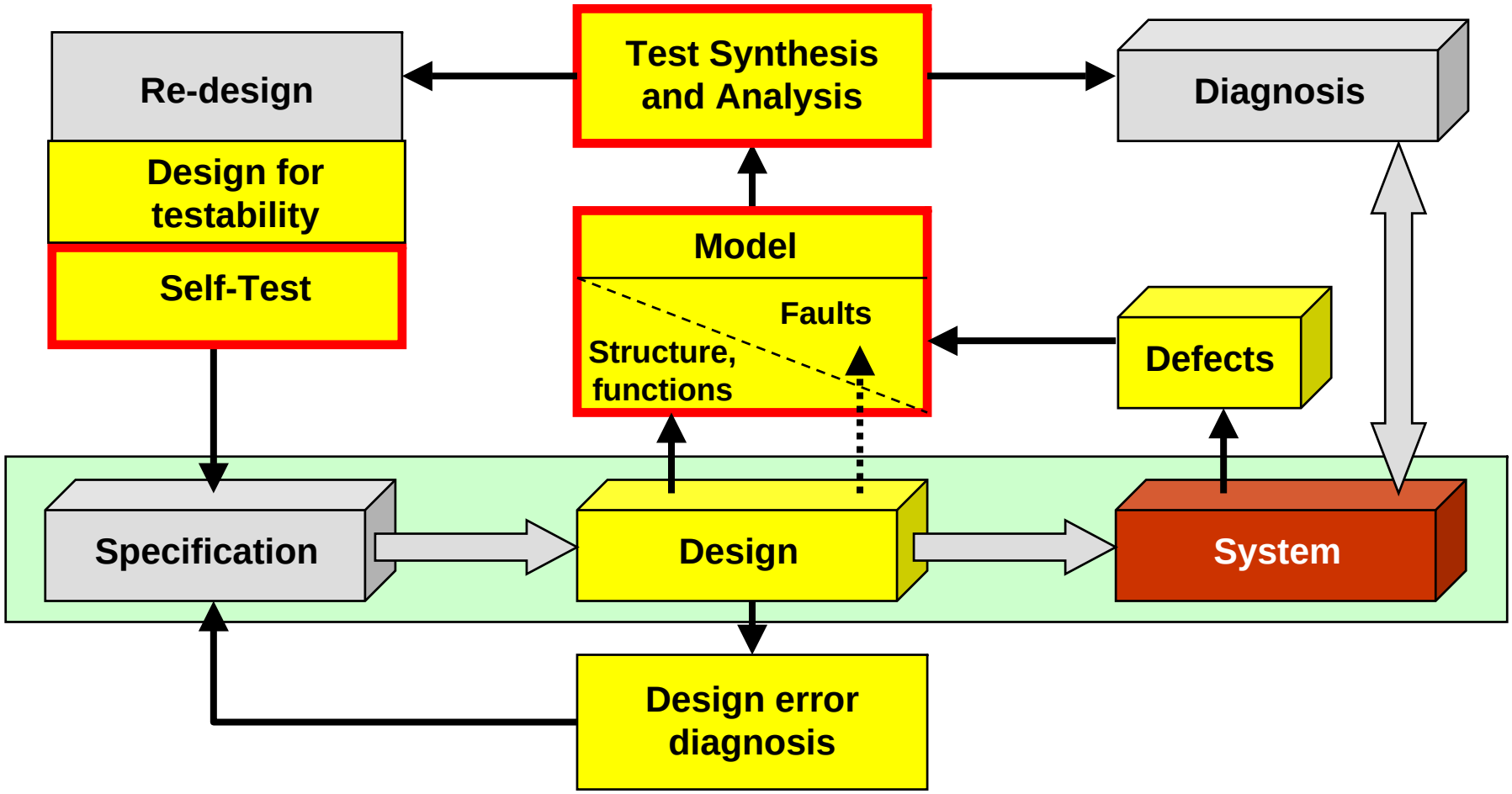
WP4: Main Goals

- To strengthen and support R&D activities in Design & Test of Digital systems
- Implementation of new research results as innovative tools in the local industry
- Creation of a multi-functional CAD environment
- To strengthen international research contacts via mutual cooperation

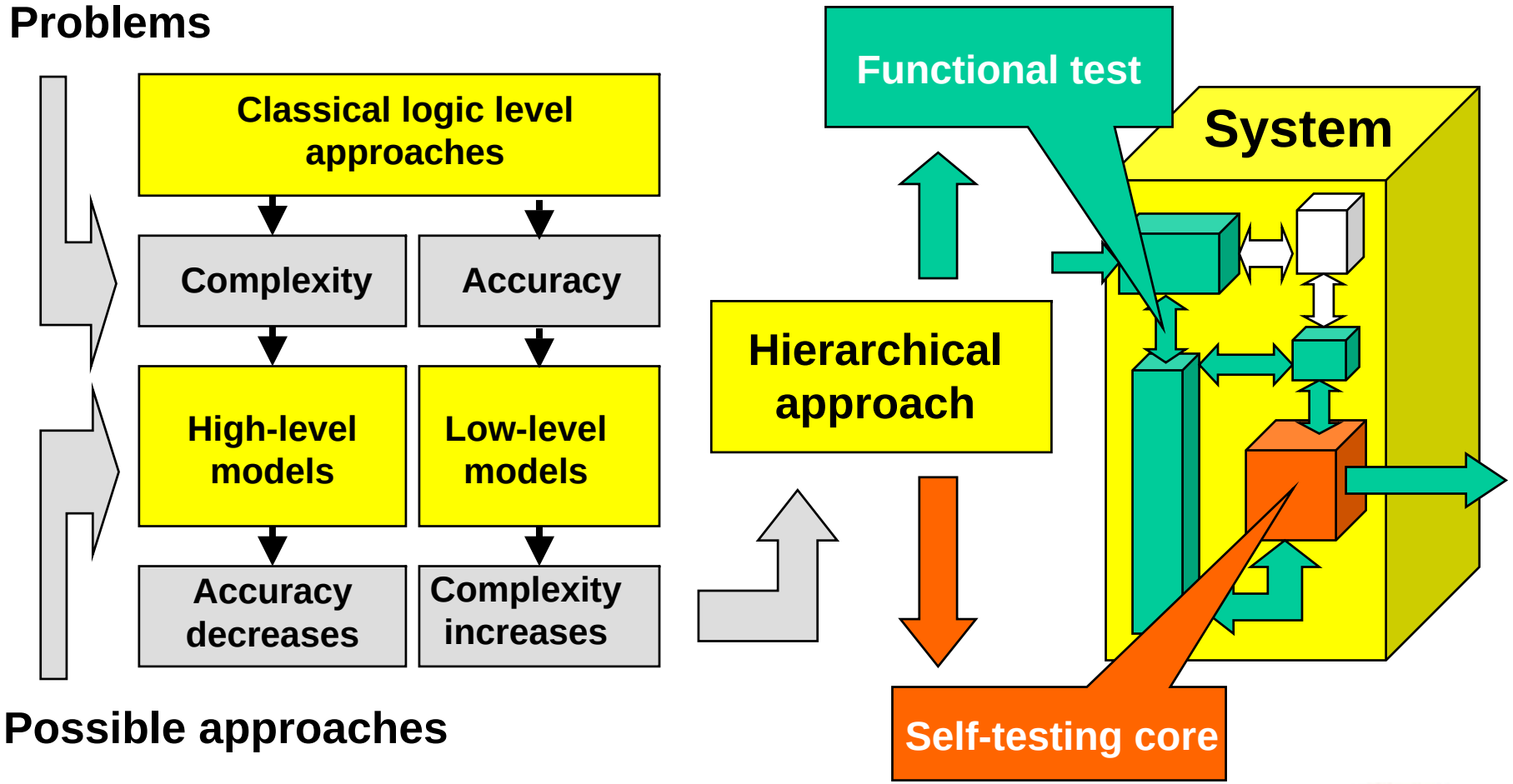
Content

- Research overview
- Multifunctional CAD environment
- Deliverables
- International cooperation
- Self-assessment
- Exploitation plans
- Conclusions

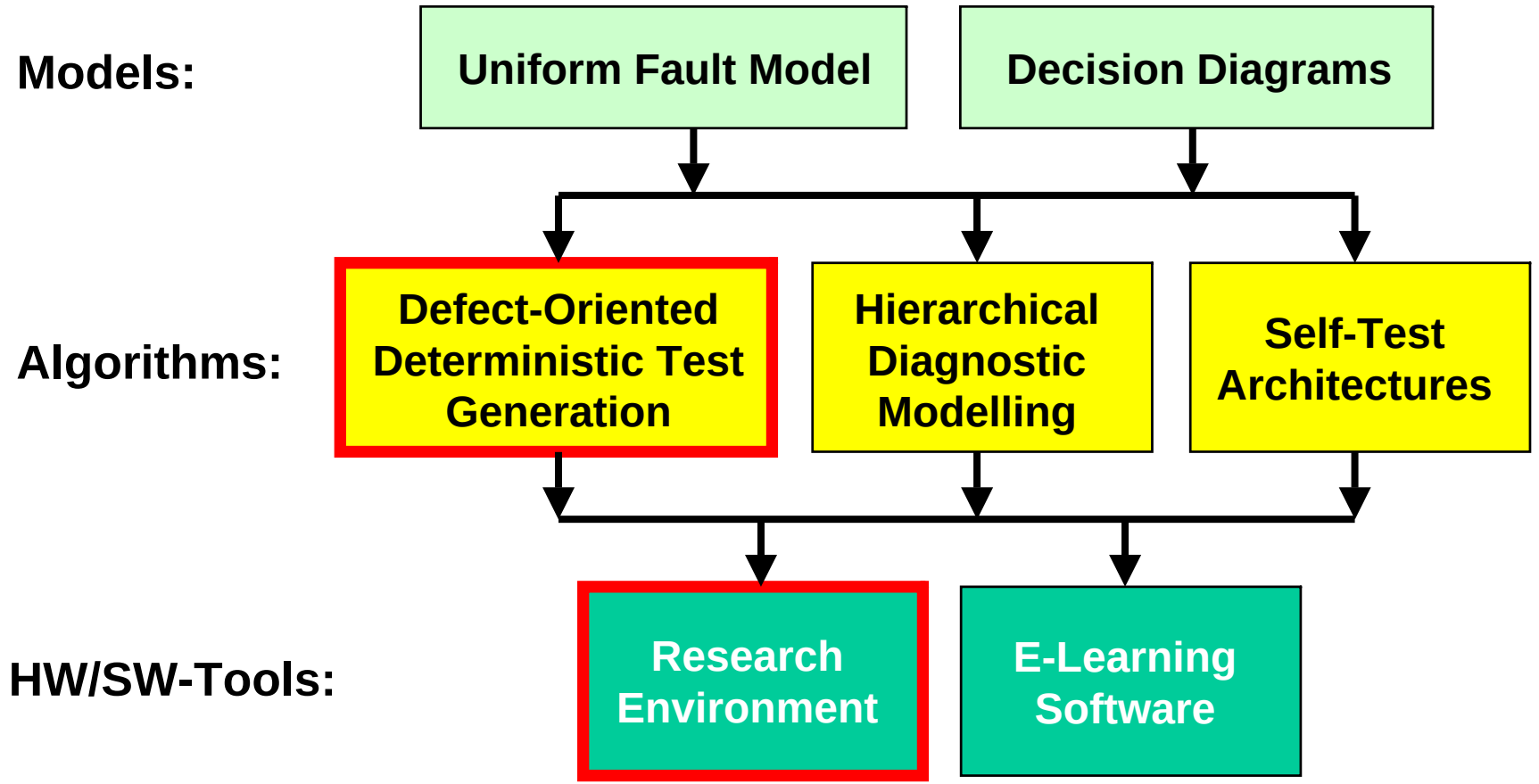
The Map of Research Topics



Research Problems and Motivations



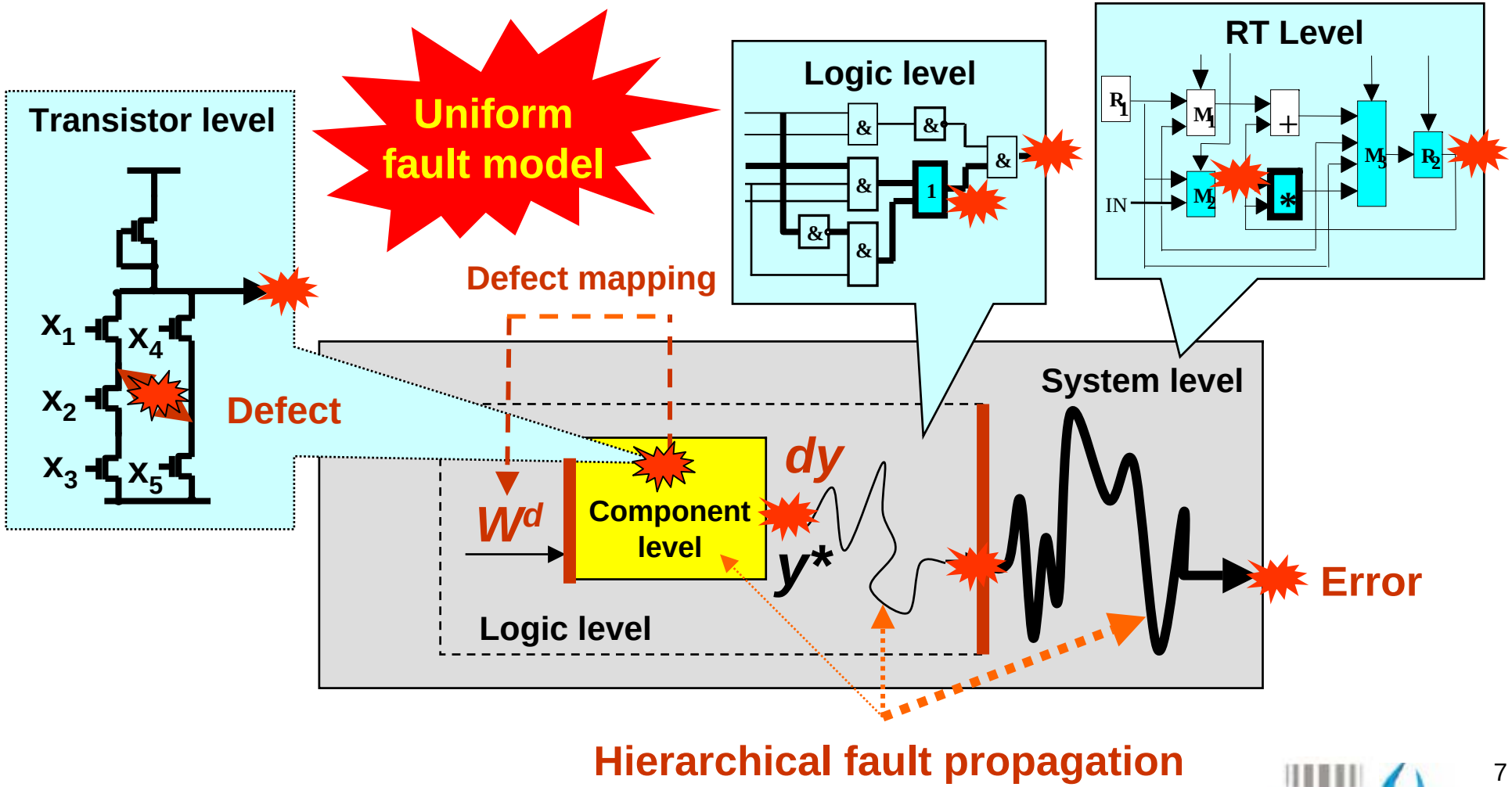
Research Activities in 2003-2005



Research Results in 2003-2005

- **Uniform fault model**
  - for diagnostic analysis of digital systems at different abstraction levels
- **Defect-oriented deterministic test generator**
  - such a tool is missing in the world
- **Hierarchical diagnostic modelling of digital systems**
  - to increase the modelling speed and accuracy
- **HW-based SW-solutions with reconfigurable logic**
  - speed of fault simulation increased more than 200 times
- **Self-test in systems**
  - new optimization algorithms
  - criteria: time ↓, H/W cost ↓, power consumption ↓, quality of testing ↑
- **Multifunctional research environment**

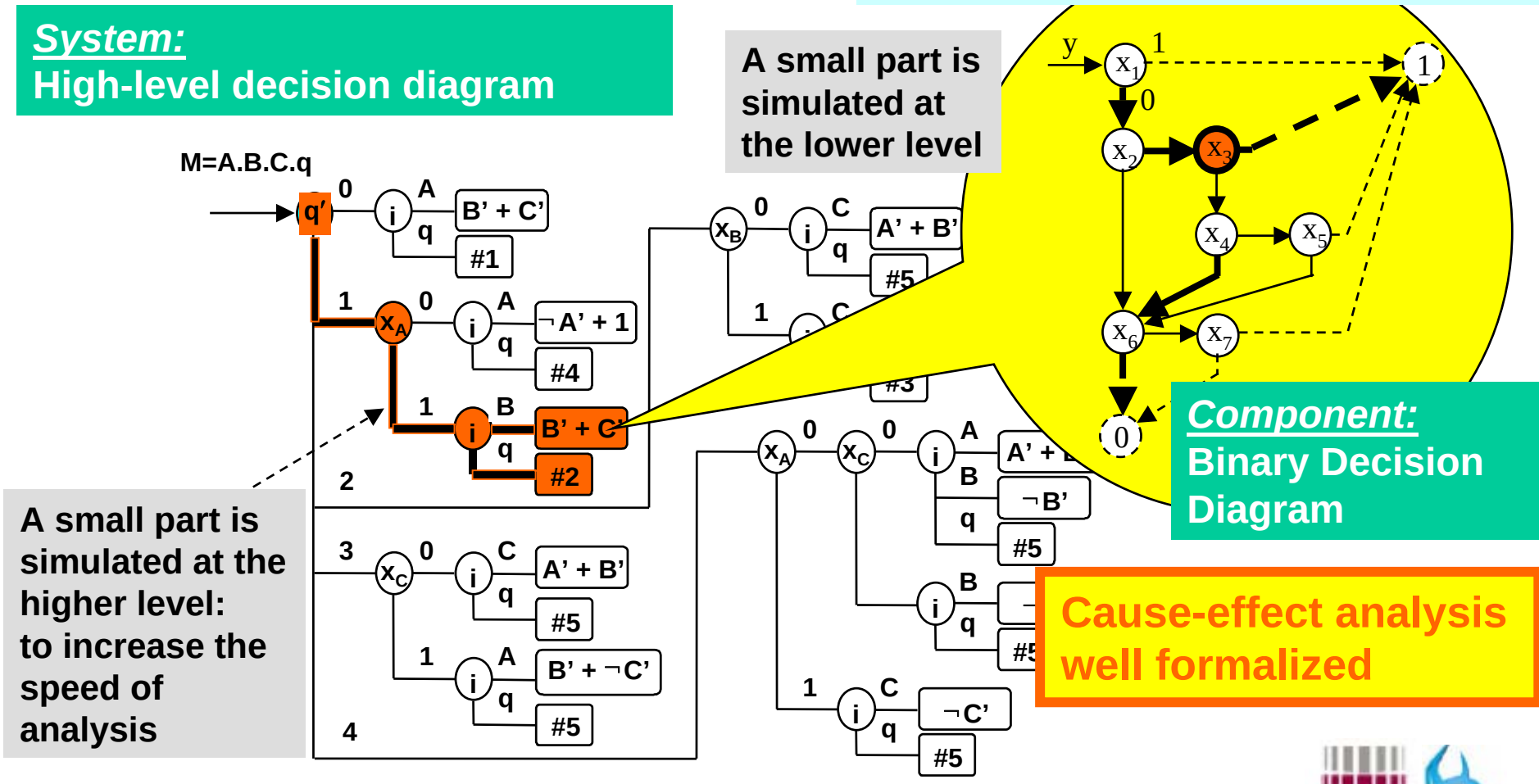
Hierarchical Diagnostic Modeling



Hierarchical Diagnostic Modeling by DDs

Cooperation: **Tartu University**

System:
High-level decision diagram



A small part is simulated at the lower level

A small part is simulated at the higher level: to increase the speed of analysis

Component:
Binary Decision Diagram

Cause-effect analysis well formalized

Defect-Oriented Test Generator

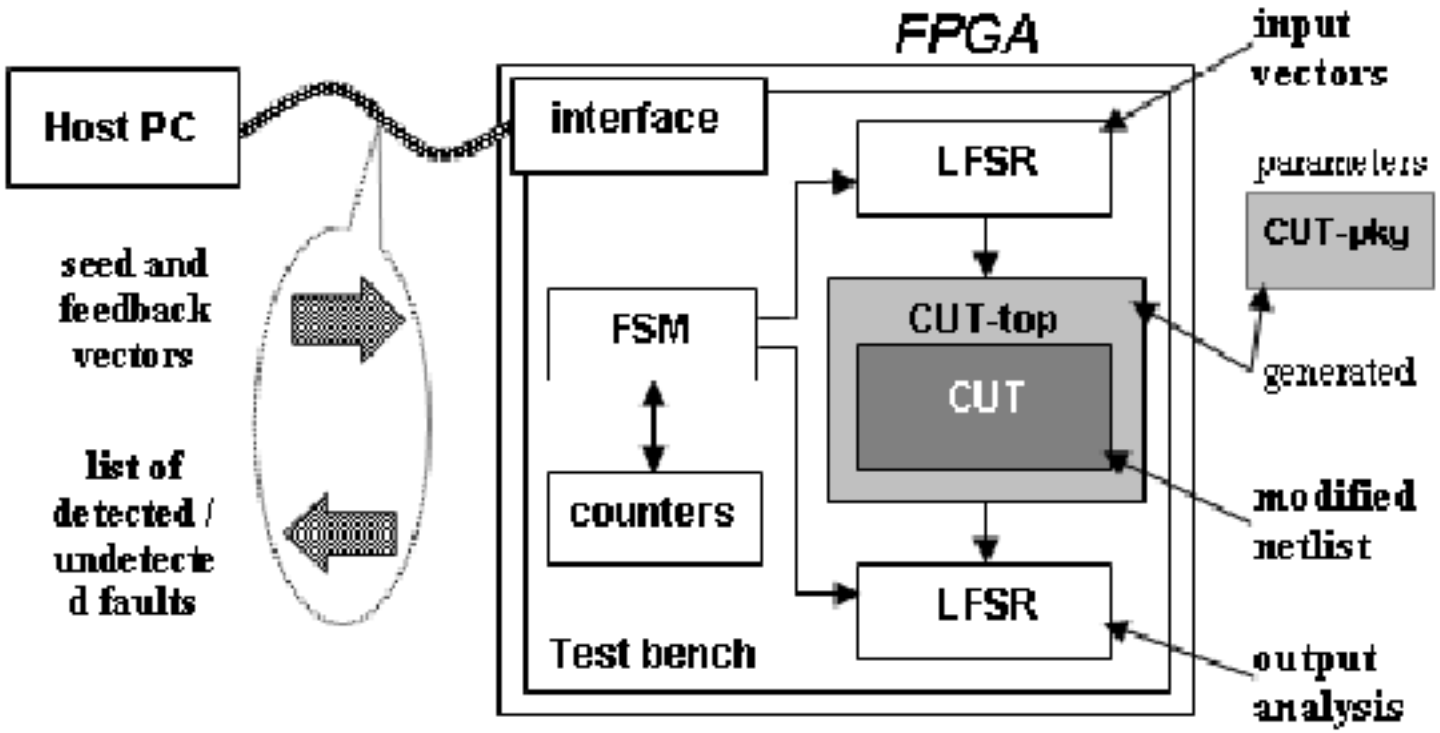
Cooperation: **TU Darmstadt, TU Warsaw**

Circuit	Number of defects			Defect coverage			
	All defects	Redundant defects		100% stuck-at fault ATPG			DOT
		Gates	System				
1	2	3	4	5	6	7	8
c432	1519	226	0	78,6	99,05	99,05	100,00
c880	3380	499	5	75,0	99,50	99,66	100,00
c2670	6090	703	61	79,1	98,29	98,29	100,00
c3540	7660	985	74	80,1	98,52	99,76	99,97
c5315	14794	1546	260	82,4	97,73	99,93	100,00
c6288	24433	4005	41	77,0	99,81	100,00	100,00

Method for proving the redundancy of defects

Surprising new result: very high redundancy of defects

Accelerators With Reconfigurable Logic

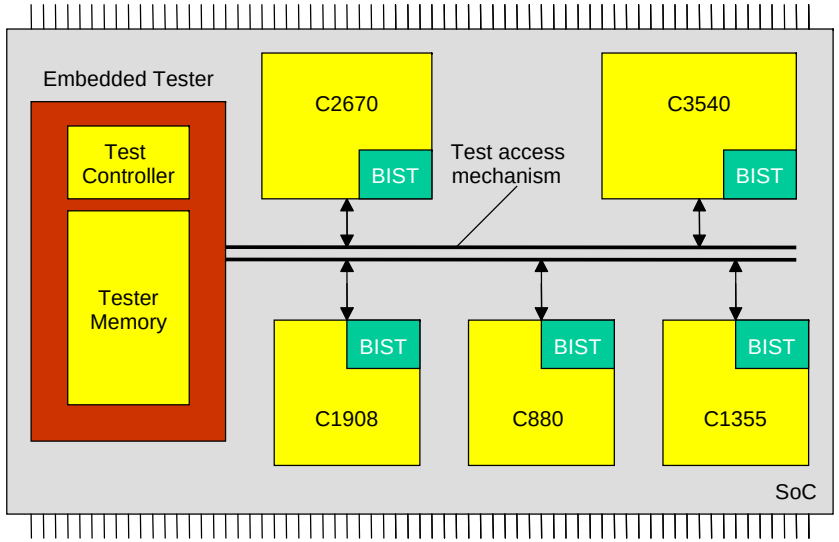


Fault simulator tool is implemented as hardware

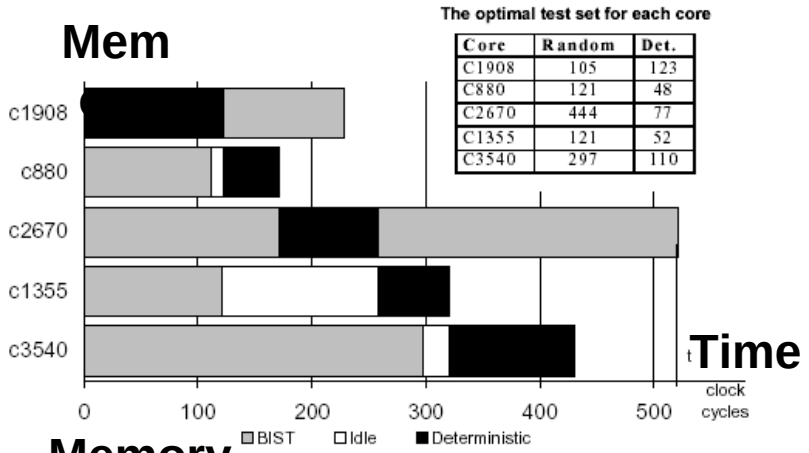
The speed of fault simulation was increased more than 200 times

Hybrid Built-In Self-Test

Parallel-sequential testing:



Cooperation: **Linköping University**

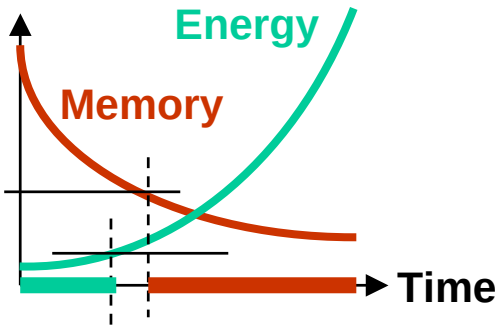


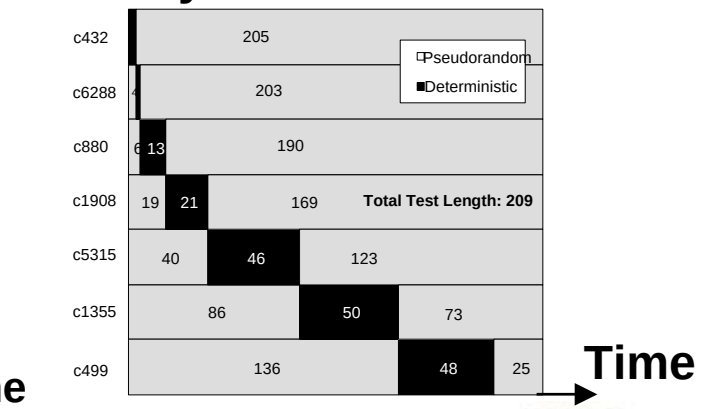
The optimal test set for each core

Core	Random	Det.
C1908	105	123
C880	121	48
C2670	444	77
C1355	121	52
C3540	297	110

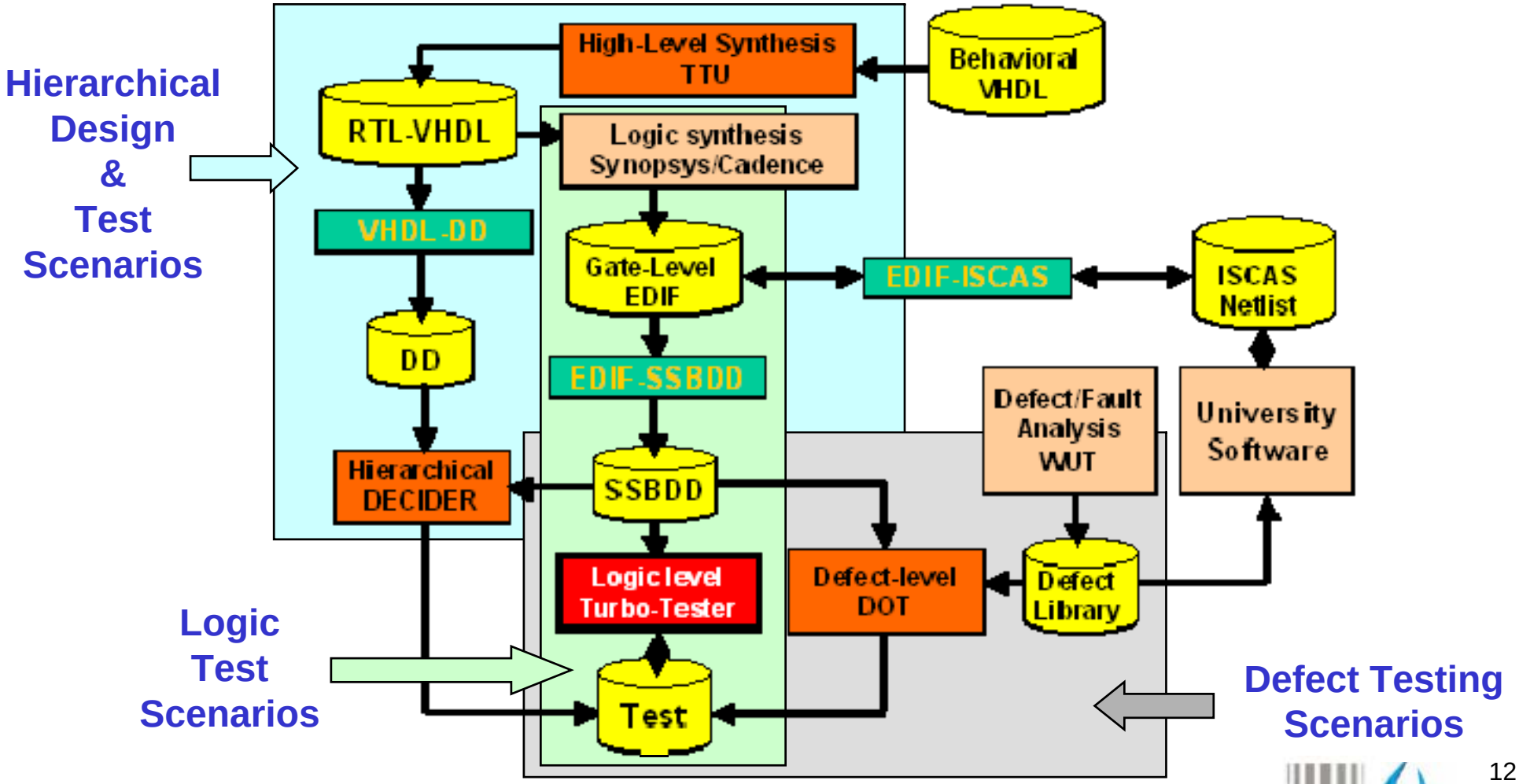
Optimization:

- **testing time ↓**
- **memory cost ↓**
- **power consumption ↓**
- **hardware cost ↓**
- **test quality ↑**



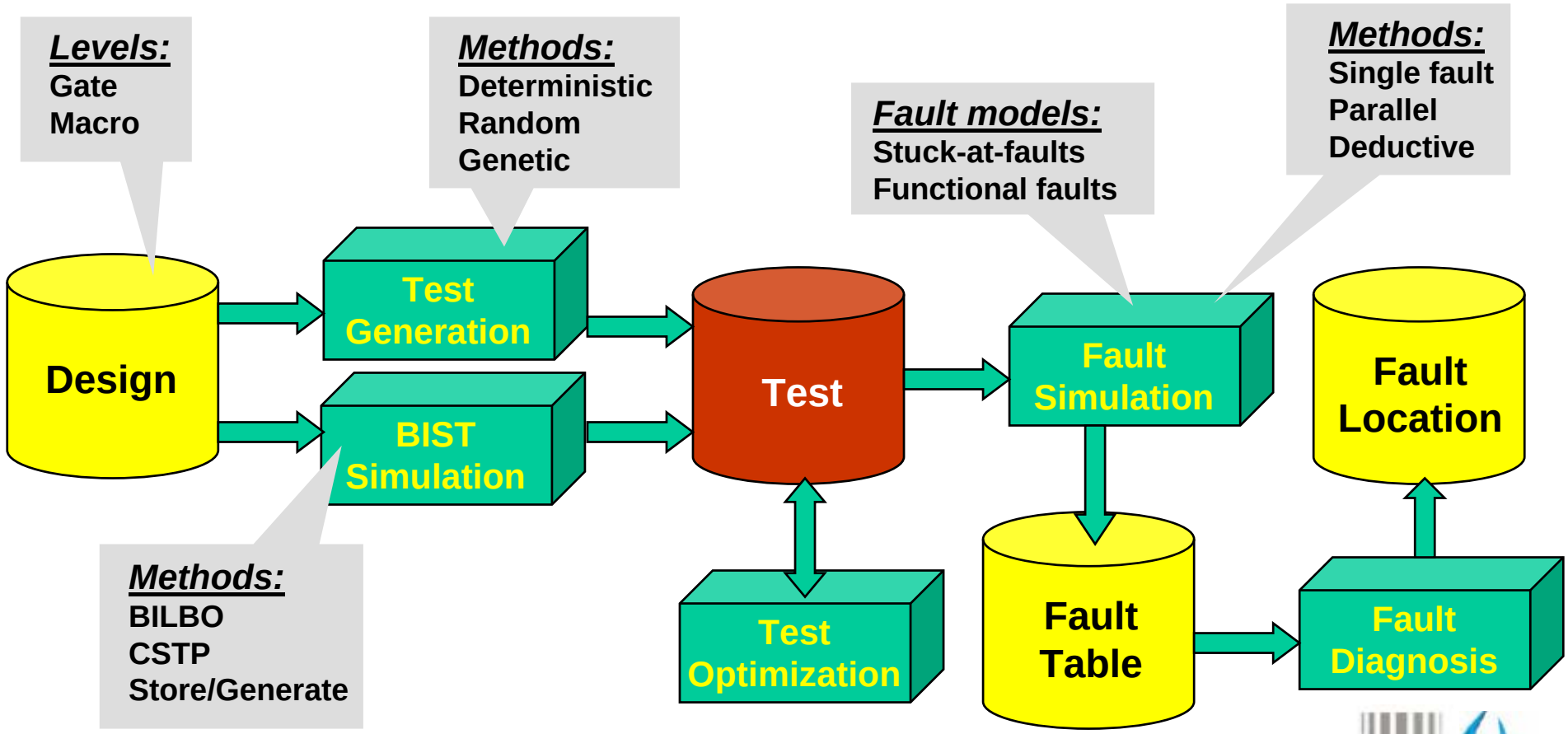


Multi-Functional CAD Research Environment

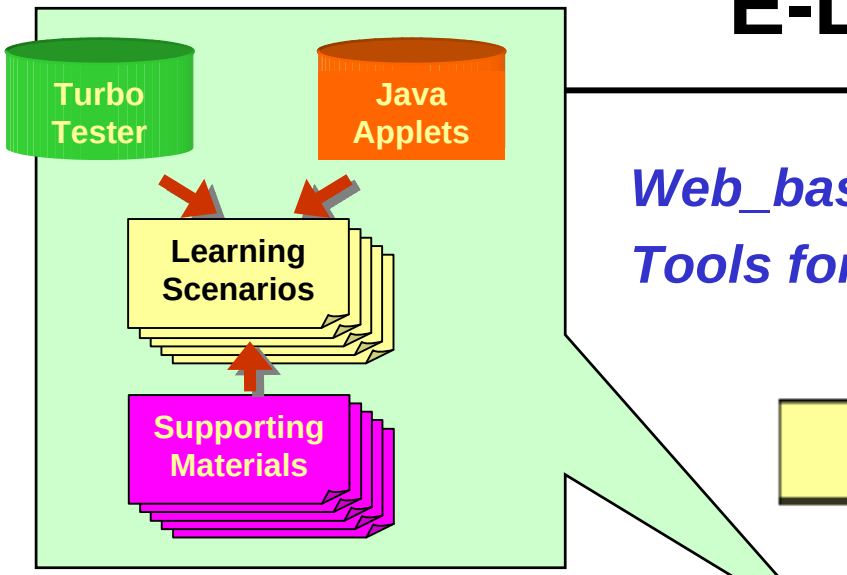


Multi-Functional CAD Research Environment

TURBO-TESTER: **Used in >90 institutions in >30 countries**

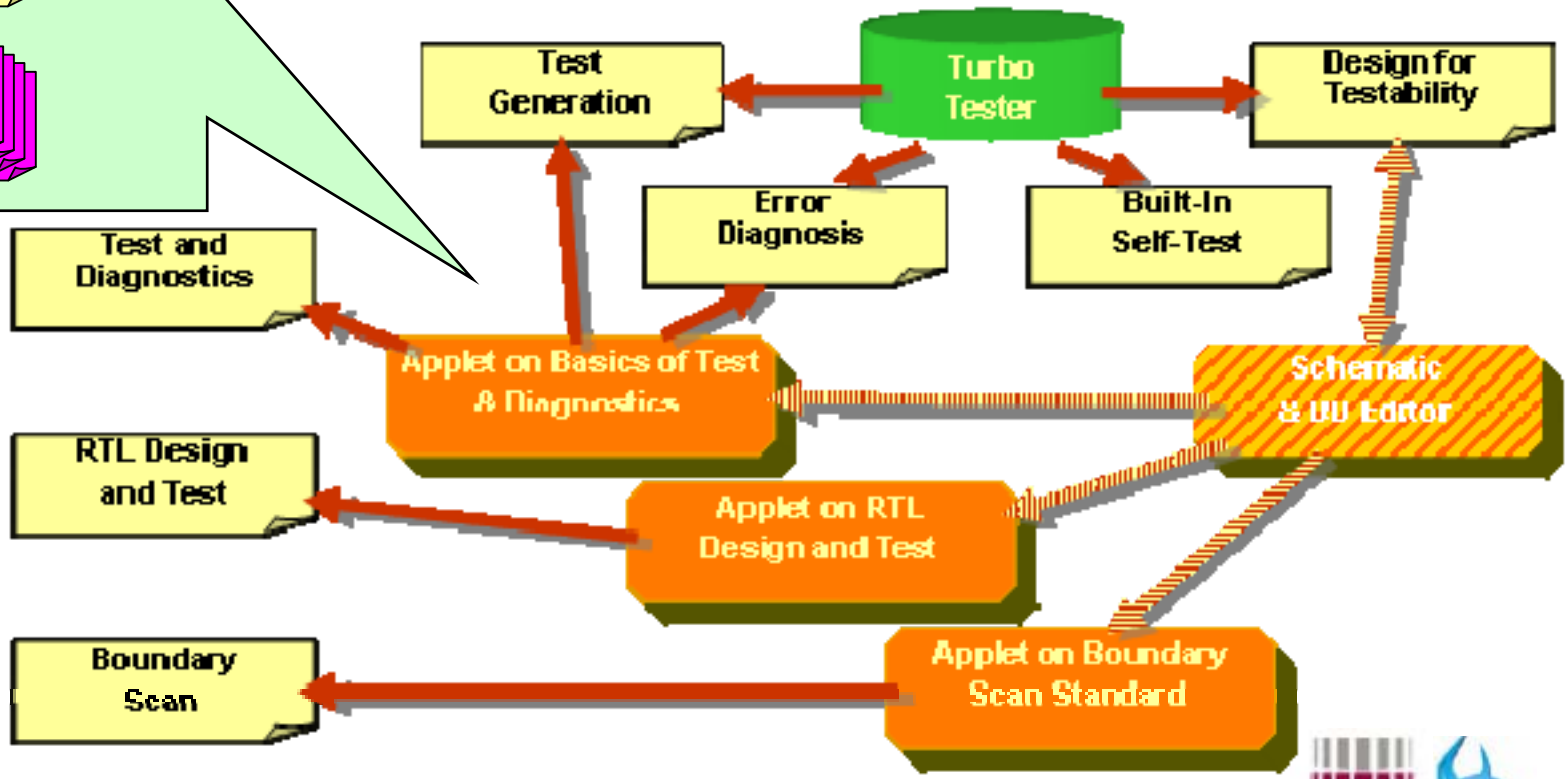


E-Learning Software



Web_based tools for classroom, home and exams

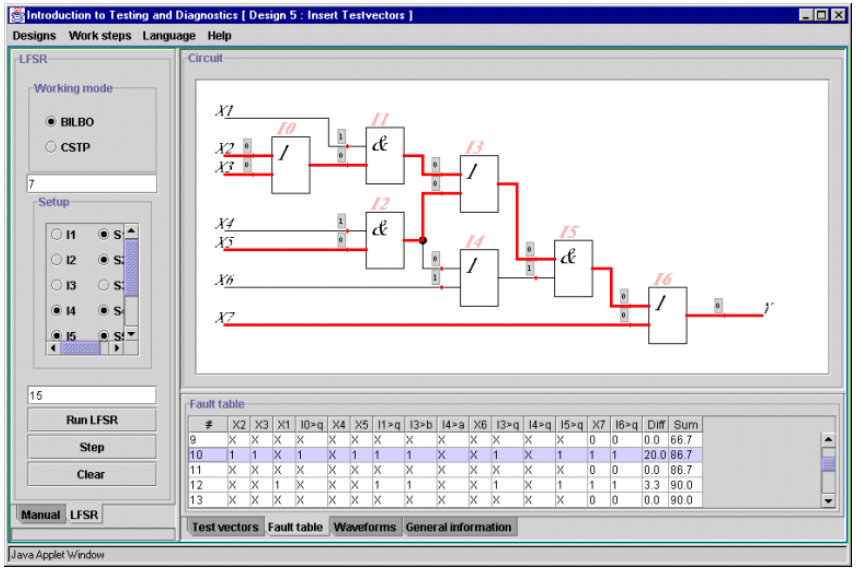
Tools for laboratory research



E-Learning Software

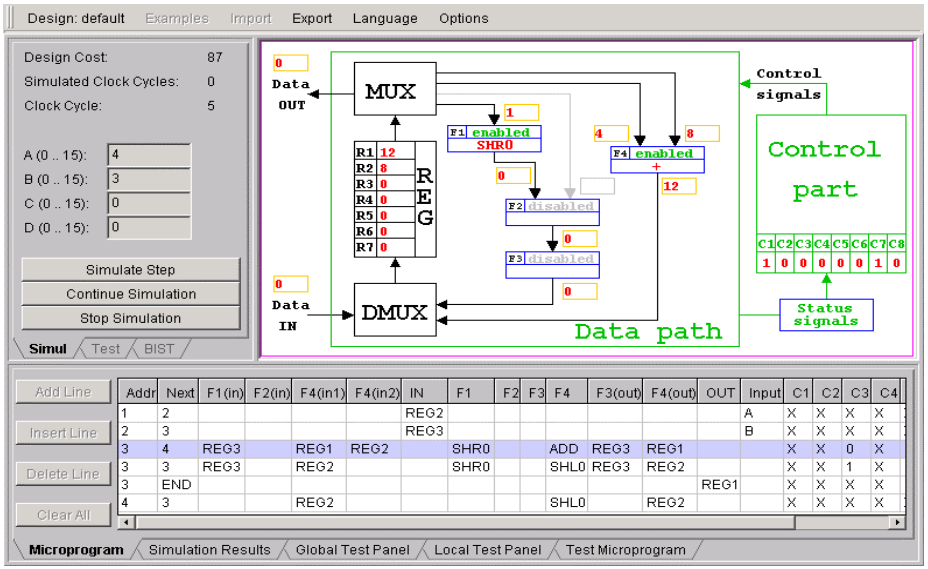
Java applets for classroom, home, labs and exams:

Logic level diagnostics



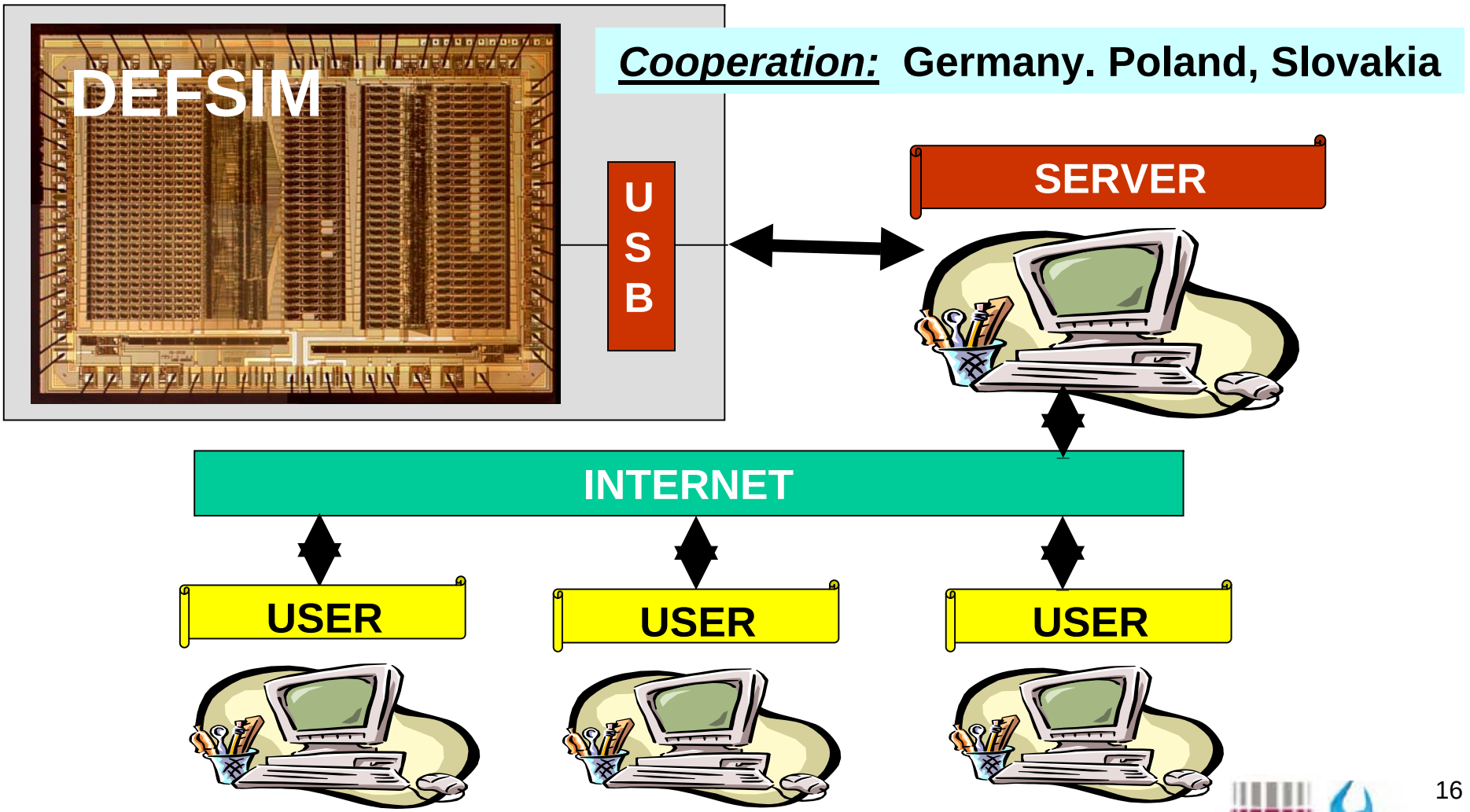
Cooperation: **TU Ilmenau**

System level diagnostics



Other applets: Boundary Scan

Defect Investigation Environment



Cooperation: **Germany. Poland, Slovakia**

Deliverables: International conferences

D4.2. Three international workshops were planned

- **1st East-West Design and Test Workshop - EWD&TW'03**
  - **Sept 17-21, 2003 in Alushta (Ukraine) in cooper. with Kharkow National University of Radioelectronics (KNURE)**
- **2nd IEEE East-West Design and Test Workshop - EWD&TW'04**
  - **Sept 23-26, 2004, in Alushta (Ukraine) in cooper. with KNURE**
- **9th Baltic Electronics Conference – BEC'2004**
  - **Oct 4-6, 2004, in Tallinn**
- **10th IEEE European Test Symposium – ETS'05**
  - **May 22-25, 2005, in Tallinn. A great (154 papers submitted, only 31 accepted**
  - **Two of the papers from the researchers of TTU**
  - **The total number of participants was more than 200, which was the record in the history of ETS**
- **4th IEEE European Board test Workshop – EBTW'05**
  - **May 25-26, 2005 in Tallinn**
- **3rd IEEE East West Design & Test Workshop - EWD&TW'05**
  - **Sep 15-19, 2005 in Odessa in cooper. with local organizers KNURE**

Deliveables: Numbers and Facts

D4.1. New courses (2)

- Digital Test
- Design for Testability

D4.3. Publications (30 was planned)

- 15 journal papers, 3 books and 7 chapters in books
- 80 conference papers

D4.6. Participation in conferences (10 was planned)

- 74 papers at 34 conferences, 6 symposia and 10 workshops
- 3 Best Paper Awards, 2 invitations to plenary sessions

D4.8. Presentations of Estonian RTD results in SoC

- 24 (74) presentations at conferences
- 13 (32) presentations at seminars and tutorials

Deliverables

D4.4. Roadmap report

Semiconductor Technology, Dersign and Test Roadmap

- **The main implication of the roadmap is that**
  - **design costs are rapidly growing and**
  - **test is taking an ever increasing part of them**
- **Thus,**
  - **more powerful test and design for testability methods are needed to be applied in Estonia and globally in order to**
  - **increase designer's productivity and thereby bring down the costs**
- **Two publications were written on this topic for popular science IT journals:**
  - **J.Raik. Semiconductor Industry Roadmap until 2016: A Futue Vision of Chip Technology, Design and Test). A&A, TTU press, No. 6, 2003, pp. 9-16**
  - **J. Raik. Chip design and test in the Baltics: Fact or Fiction. Baltic IT&T Review. (to be published)**

Deliverables

D4.5. Studies on different topics

- Studies on Decision Diagrams and logic testing
  - Development of chapters of a course “Digital test”
- Studies on testing of System-on-chips
  - Built-In Self-Test and Design for Testability issues
  - Dvelopment of the course “Design for testability” (D4.1a)
- Testing Strategies of SoC
  - Defect-oriented testing and hierarchical testing
  - Dvelopment of the course “Digital test” (D4.1b)
- High-Level synthesis
  - Development of a course on VLSI design and high-level synthesis

D4.7. Reviews of the Advisory Board

- The number of the AB members – 7
- 7 reviews for 2 annual reports of 2003 and 2004
- All reviews were positive

Student Placements & Cooperation

D4.9. Study visits of students

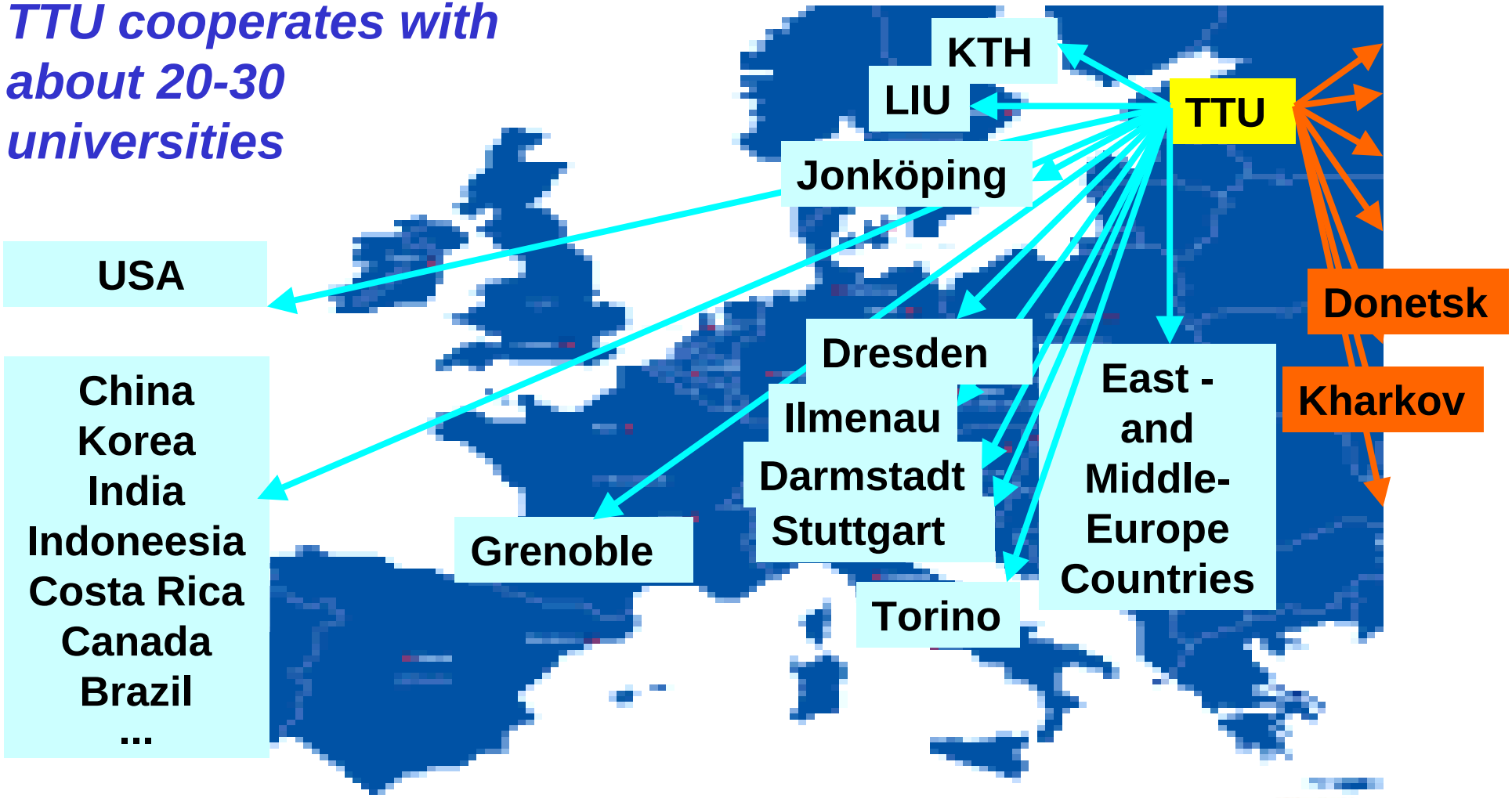
- **TU Ilmenau (Subcontractor S16): 8 students, 21 months**
  Results: **web-based teaching environment**
- **Linköping university (Subcontractor S14): 2 students, 6 months**
  Results: **12 joint research papers**
- **Three students (KTH Stockholm, TU Darmstadt, Tartu University) at TU Tallinn**
  Results: **6 joint papers and 2 MSc thesis**

D4.10. Practical placements in industry

- **Fraunhofer Institute for IC (Subcontractor 15, Dresden, Germany) – 1 student, 2 months**
  Results: **web-based teaching environment, 2 joint papers**
- **Artec Design company, Estonia (Subcontractor 13) – 1 student, 2 months**
  Results: **2 contracts and joint cooperation, testing our research results for industrial products**

Cooperation: Research & Teaching

TTU cooperates with about 20-30 universities



Cooperation with Industry

International cooperation

- **Cooperational links to:**

  JTAG Technologies, National Instruments, DIGSIM DATA (in Sweden), Fraunhofer Institute of IC (in Germany), Insight Memex/Xilinx (in France)

  3 tutorials were carried out by the representatives of these companies
- **Ericsson AB, SAAB (Sweden) – contract negotiations ongoing for development of support software for new standards of Boundary Scan (I-JTAG and S-JTAG)**
- **Fraunhofer Institute of IC (in Germany) – our ATPG tools were used for an industrial product, joint development of web-based collaborative design environment MOSCITO, 3 placements**
- **DIGSIM DATA (Sweden) – exchange of tools for teaching (dixiCAD vs. TT)**
- **JTAG Technologies (Finland) – joint lecturing in tutorials, they are using our BSCAN-applet in their courses**

Cooperation with Industry

Cooperation in Estonia

- **Cooperational links to: Artec Design, Elcoteq Network Corp., Analog Design AS, Liewenthal, Elvior, M&T Electronics, Cybernetica AS, Borthwick Pignon, AS MicroLink, National Semiconductor Estonia, Testset, Testonica Lab**

  10 tutorials or seminars either by experts from West (Finland, Germany, UK, France etc.) or by experts of our group to the engineers of these companies
- **Artec Design – new BIST concept used for new SoC developments, 1 placement, joint lecturing in tutorials**
- **ELIKO – Development Centre of Mission Critical Embedded Systems created (with contracts between 7 private companies)**
- **Testonica Lab – new spin-off company, contract negotiations with SAAB and Ericsson AB (Sweden), joint development of test tools**

Academic International Cooperation

- WP4 has cooperated with more than 20 academic institutions from 11 countries (USA, Germany, Sweden, Denmark, Czech Republic, Slovakia, Poland, Bulgaria, Russia, Ukraina and Byelorussia)
- Study visits of 10 Students (27 months in total) – TU Ilmenau, Linköping U

Teaching

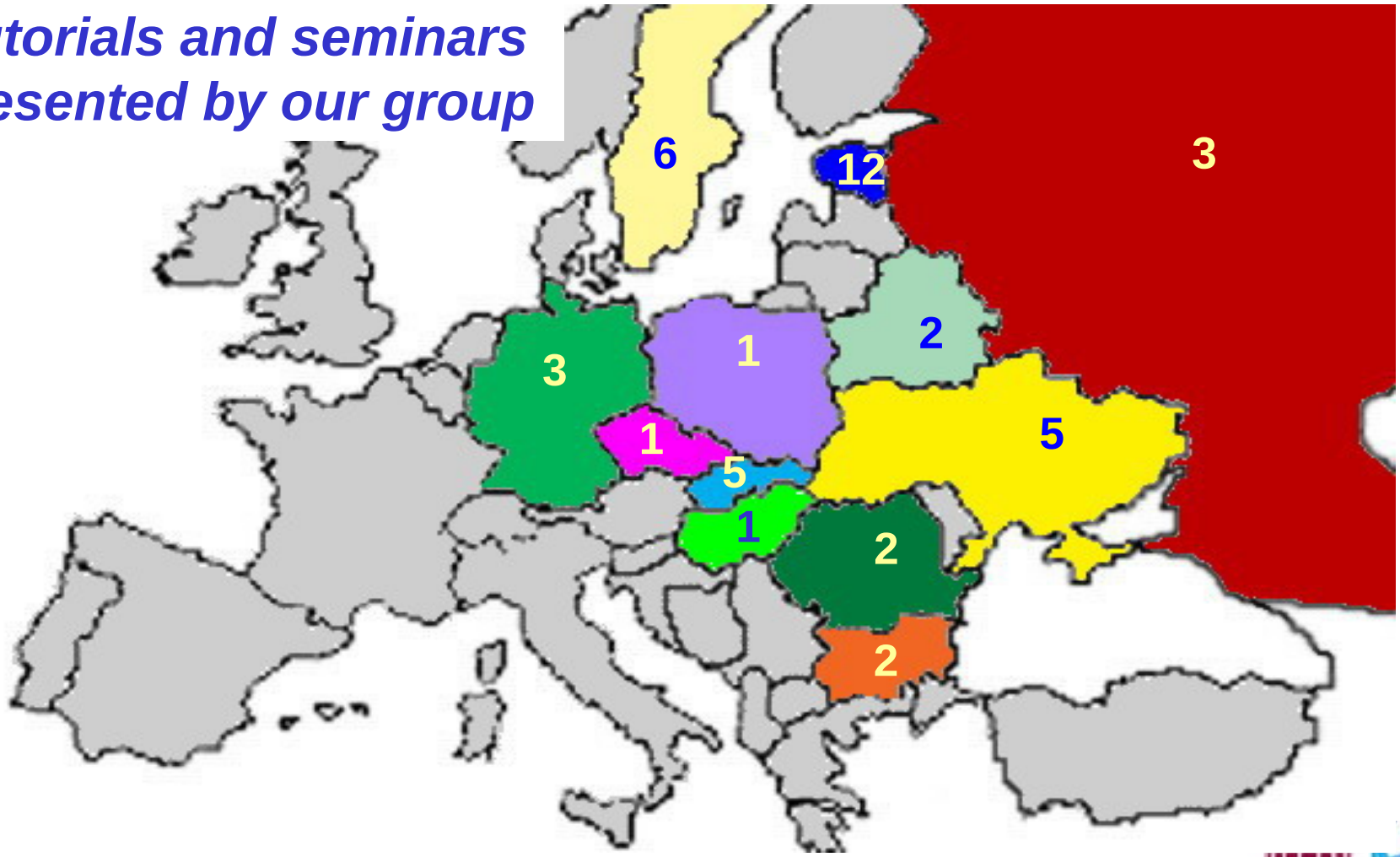
- 6 courses (32 h) at TU Darmstadt and U Jönköping (2003-2005)
- Tutorials and seminars (25 times in 10 countries)

Research

- E-Learning Environment – TU Ilmenau, Slovak Acad. of Sc (10 papers)
- DOT and joint research – TU Darmstadt, TU Warsaw (5 papers)
- BIST research – Linköping U (10 papers)
- Interconnect test – Jönköping University (2 papers)
- Test algorithms – Universities in Tomsk (Russia), Kharkov, Donetsk (Ukraine) – 6 papers
- 50 joint papers in total with 35 researchers from 11 countries

Dissemination of Results

Tutorials and seminars presented by our group



Geography of Guest-Lecturers

Academic International Cooperation

New VI Framework project proposals submitted:

- **FP6-2005-IST-5 STREP/STIP**
  Verification and Validation of Embedded System Design Workbench
  Participant contries: France, UK, Italy (2), Sweden, Estonia
- **FP6-2002-IST-C FET**
  Error Correction and Fault Repair for Network-on-Chip based Systems – ECON
  Participant contries: Germany, Sweden, Italy, Estonia
- **FP6-2005-IST-5 STREP**
  Adaptable Interconnect-centric Multiprocessor Embedded Systems -AdaptIn'
  Participant contries: Germany (3), France (2), Sweden, Finland, Brazil, Estonia
- **FP6-2005-IST-C 2.3.4.1 FET Open STREP**
  Error-Tolerant Multiprocessor Nanoelectronics Systems – ETMNS
  Participant contries: Germany (2), Sweden, Finland (2), Estonia

Cooperation with 16 institutions from 7 countries, incl. 5 companies

Self-assessment: Most Important Results

Research

- New joint research directions and cooperations were launched
  - Defect-oriented test (DOT – the first tool able to prove redundancy of defects)
  - HW emulation of SW algorithms (Accelerator for fault simulation – 200 times faster)
- Improvement of the research potential
  - 3 PhD thesis was defended in 2003-2005
  - 1 team member returned with PhD degree from Sweden
- Advanced multifunctional lab environment
  - allows effective teaching and collaboration between partners in research
  - TT tool set is used in 90 institutions in 30 countries

Teaching

- Strong impact of the project in improving the level of teaching
- New courses and tools created and introduced into teaching
  - Courses and tools have received a broad international recognition
  - 6 courses were given in Germany and Sweden (2003-2005)

Self-assessment: Important Results

New local structures created

- **Development Centre ELIKO (involving 7 SMEs)**
- **New company Testonica Lab**

International cooperation

- **Organization of 6 conferences or workshops**
- **About 50 joint papers with 35 researchers from 18 academic institutions of 11 countries**
- **Mutual knowledge transfer between West and East (seminars, reviewing PhD thesis, guest lecturing, research visits)**
- **Cooperation with Eurotraining – distribution of our tools in Europe**
- **New research consortiums: 4 VI Framework project proposals with 16 institutions (5 companies) from 7 countries were submitted**

Exploitation plans

- **A SW/HW based research environment offers a lot of opportunities to continue cooperation between partners - Linköping U, TU Darmstadt, TU Ilmenau, KTH Stockholm, Fraunhofer Institute of IC Dresden, Politecnico di Torino etc.**
- **International cooperation in teaching will be extended. The new tools will be made available via the framework of EuroTraining "Microsystems University Service" action**
- **SMEs will be involved in the R&D based on the created environment - ELIKO, Artec Design, Testonica**
- **Further research will target the activities of I-JTAG and S-JTAG related to the new standards of Boundary Scan in cooperation with western industry - Ericsson, SAAB**

Conclusions

- All the initial targets and goals of WP4 were reached
- The project allowed to
  - improve the level of teaching, and to
  - push future research in form of a broad international cooperation
- Working connections (cooperation, contracts, joint centres) to industry were created
- New multifunctional lab research environment was developed which serves as an incubator of new research and pedagogical ideas
- The project had an impact (knowledge transfer) in 2 directions: West-to-East, East-to-West

A lot of thanks to the Project Coordinator and to the whole eVikings Project Team!