Electronics Design and Test

International User Forum

Tallinn, October 11, 2000

Virtual R&D Laboratory

A European Project

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Partners of the project

- Fraunhofer Institute for Integrated Circuits, Dresden (coordinator)
- TU Budapest (scientific coordinator)
- TU Darmstadt
- Linköping University
- Institute of Informatics, Bratislava
- Slovak Technical University, Bratislava
- Institute of Electron Technology, Warsaw
- Warsaw University of Technology
- TU Tallinn

Mission of the project

- **Virtual Laboratory will offer a new quality in _cooperative_ R&D and teaching**
- **Partners**
  - **are _sharing_ software tools and courses**
  - **carry out _joint work_ on research subprojects and designs**
  - **provide _mutual access_ to microelectronics component libraries, benchmark circuits, design examples etc. available at partners**
  - **serve as a source of information to interested institutions, including national industries with a special emphasis on SMEs**
- **For these purposes Internet-based tools and organizational procedures will be developed.**

Mission of the project

- **Three lines of complementary actions are foreseen:**
  - setting up a research environment,
  - cooperative R&D and teaching activities supported by virtual resources
  - making the R&D results visible to the outside world by organizing User Forums and publishing regularly electronic newsletters
- **Scientific mission of VL is to address the challenging topics in "Design of Dependable Micro-electronics Systems" by joining scientific competence and research efforts from related fields like**
  - microelectronics design and design methodologies,
  - software/hardware co-design,
  - test generation, and diagnosis

for reaching new quality and dependability of tomorrow's systems

Working paradigm in VILAB

- For coordinating the cooperative work,
  - a system of tasks and subtasks was set up to highlight the main ideas and directions of future joint activities in the virtual environment which itself was to be created.
- The big number of partners appointed for several tasks (subtasks) made it reasonable to start at first with joint actions in smaller groups of partners
- the "format of subprojects" was introduced for carrying out cooperative work for fulfilling the tasks (subtasks)

Working paradigm in VILAB

- The whole work in VILAB can be regarded at five management levels:
  - project,
  - workpackages,
  - tasks,
  - subtasks and
  - subprojects.
- Tasks and subtasks form a “static frame” for all activities defined in the project proposal
- Subprojects being set up during the project will form a “dynamic frame” of cooperation, which is continuously developing driven

  by new growing environment possibilities and new demands

Working paradigm in VILAB

- The technique of setting up a subproject may be threefold:
  - top-down approach (initiated by a task leader),
  - bottom-up approach (initiated by at least two partners responsible for the task), or by the
  - "meet in the middle" or "yo-yo" method, where several partners together with the task leader are formulating the subproject idea
- Tasks and subtasks can be seen as the horizont towards the partners are striving
- Subprojects, on the other hand, form more precisely specified joint activities aimed on getting well-defined R&D results

Selected research results from VILAB

Creating the environment for research (Task 2)

- Fault simulation and test generation tools (*Task 2.2*)
- Interfaces between design tools and test tools (*Task 2.3*)
- Creation of the family of benchmark circuits (*Task 2.4*)

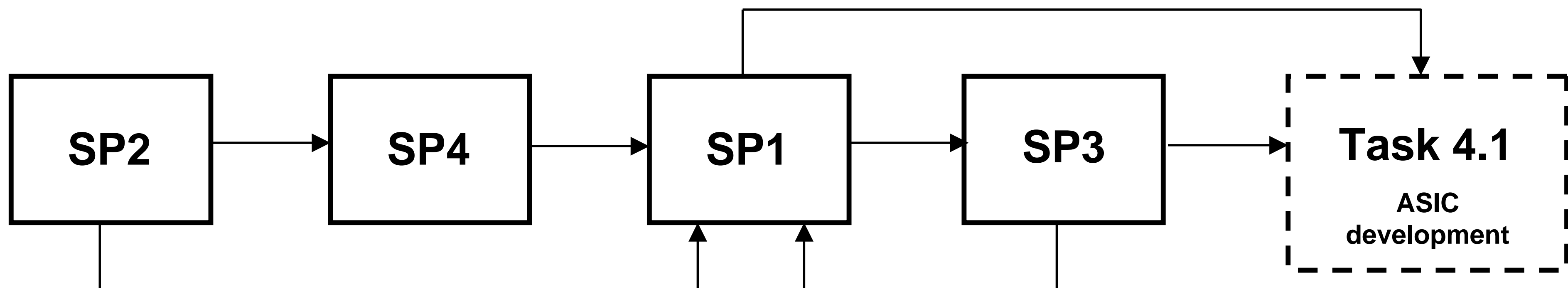
Cooperative research in DfT and Test (Task 3.1)

- FPGA design flow with test activities (*Subproject 1*)
- I_{DDQ} ATPG and testing (*Subproject 2*)
- Testability driven system design flow (*Subproject 3*)
- Defect level test analysis (*Subproject 4*)

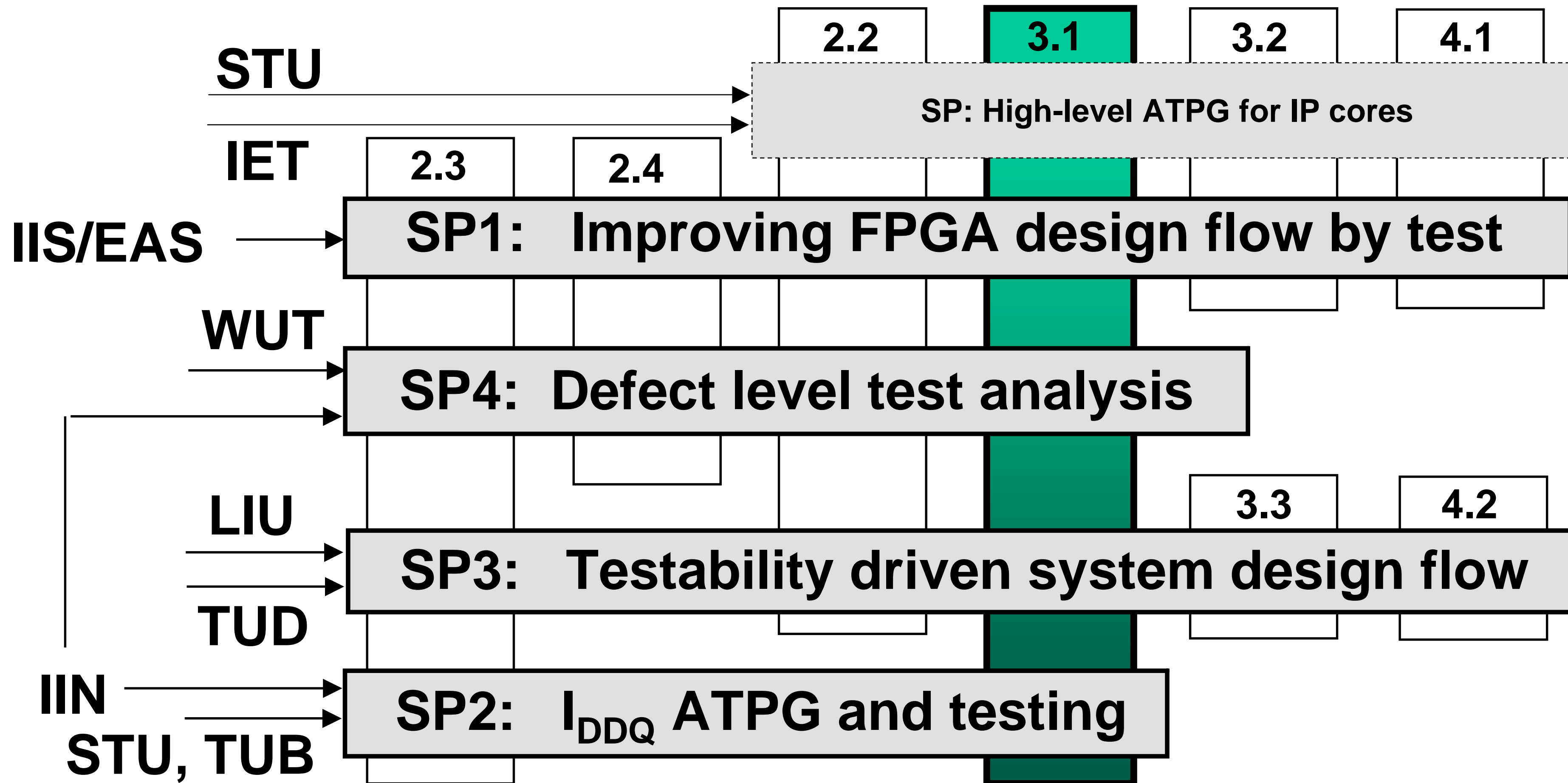
Cooperative R&D in DfT and Test Generation

Subprojects:

- **SP1: Design flow with test activities (IIS/EAS, TTU)**
- **SP2: I_{DDQ} ATPG and testing (IIN, STU, TUB, TTU)**
- **SP3: Testability driven system design flow (LIU, TUD, TTU)**
- **SP4: Defect level test analysis (WUT, IIN, TTU)**



Subtasks and subprojects



Subproject 1: Design flow with test

Subproject leader: **Tallinn Technical University, Estonia**

Partner: **Fraunhofer Institute of IC, Dresden, Germany**

Goals:

- **to develop a novel Automated Test Pattern Generator (ATPG) and integrate it with the FPGA Design Flow used at IIS/EAS**
- **to integrate with the ATPG the functions of Testability Design Adviser**

Main features of the ATPG:

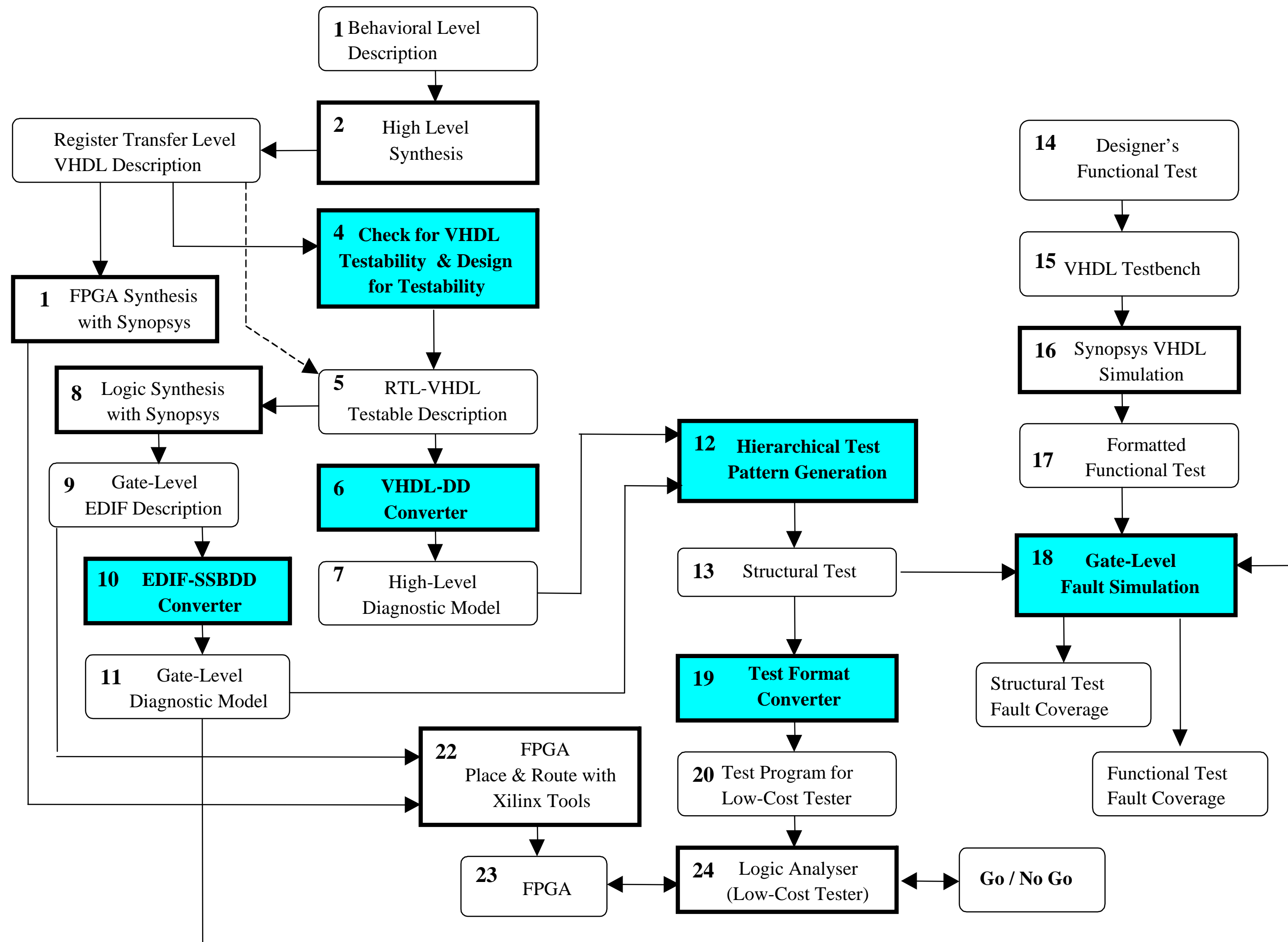
- **hierarchical approach (physical defects, gate- and RT levels)**
- **the same mathematical model for all levels - decision diagrams**
- **high speed**

Subproject 1: Design flow with test

Results:

- **Hierarchical deterministic/random ATPG - to reach high speed**
  - **which generates tests for low-level faults to reach high accuracy**
  - **by taking advantage of high-level functional (behavioural) information to reach high speed in test generation**
- **Genetic gate level ATPG - to reach high fault coverage**
- **Efficient functional simulation technique of digital systems**
- **New approaches to design error diagnosis**
  - **a method based on multiple stuck-at fault mapping to error diagnosis**
  - **diagnosis without error model**

Subproject 1: Design flow with test



Subproject 1: Design flow with test

Experimental results (ATPGs):

Circuit	Gates	Faults	States	HITEC		GATEST		DET/RAND		GENETIC	
				%	Time s	%	Time s	%	Time s	%	time s
gcd	227	844	8	89.3	196	92.2	90	91.0	3.4	93.0	702
Mult	1058	3915	8	63.5	2487	77.3	3027	79.4	13.6	80.5	19886
Diffeq	4195	15386	6	95.1	>4h	96.0	4280	95.9	80.0	97.9	53540
Huffm	2100	2816	21	12.5	16200	27.6	3553	12.5	8460	52.8	>10h

Reference ATPGs:

HITEC - T.M. Nierman, J.H. Patel, EDAC, 1991

GATEST - E.M.Rudnick et al., DAC, 1994

VILAB results:

DET/RAND - hierarchical deterministic- random ATPG

GENETIC - gate-level ATPG based on genetic algorithms

Subproject 2: I_{DDQ} ATPG and testing

Subproject leader: **Institute of Informatics, Slovak Akad. of Sciences**

Partners: **Slovak University of Technology, TU Budapest**
TU Tallinn

Goals:

- **to modify the DEFGEN ATPG system developed at II SAS**
- **to extend it by knowledge about the BIC monitor for IDDQ test application**
- **and to prove this testing methodology by its application on some experimental circuits designed by the VILAB partners**
- **The ATPG system for I_{DDQ} and/or voltage testing for combinational circuits - DEFGEN is expected to be a part of a hierarchical test pattern generator.**

SP 3: Testability driven system design flow

Subproject leader: **Linköping University, Sweden**

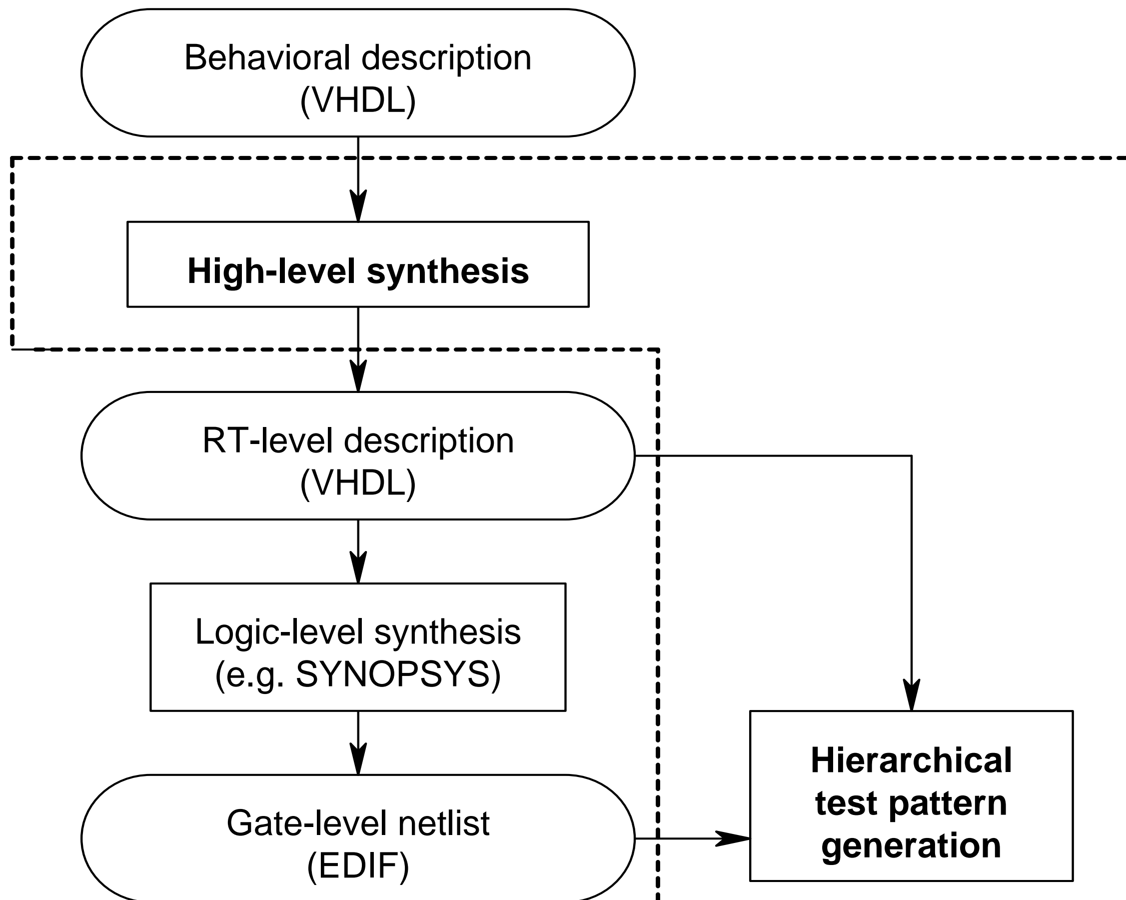
Partners: **TU Darmstadt, Germany**

TU Tallinn, Estonia

Goals:

- **to create and investigate a complete system design flow with emphasis on hardware/software partitioning, hardware testability analysis and test pattern generation, and**
- **to create a novel design and test generation system with combined High-Level Synthesis (HLS) and automated Hierarchical Test Pattern Generation (HTPG) in cooperation between Linköping University and Tallinn Technical University.**

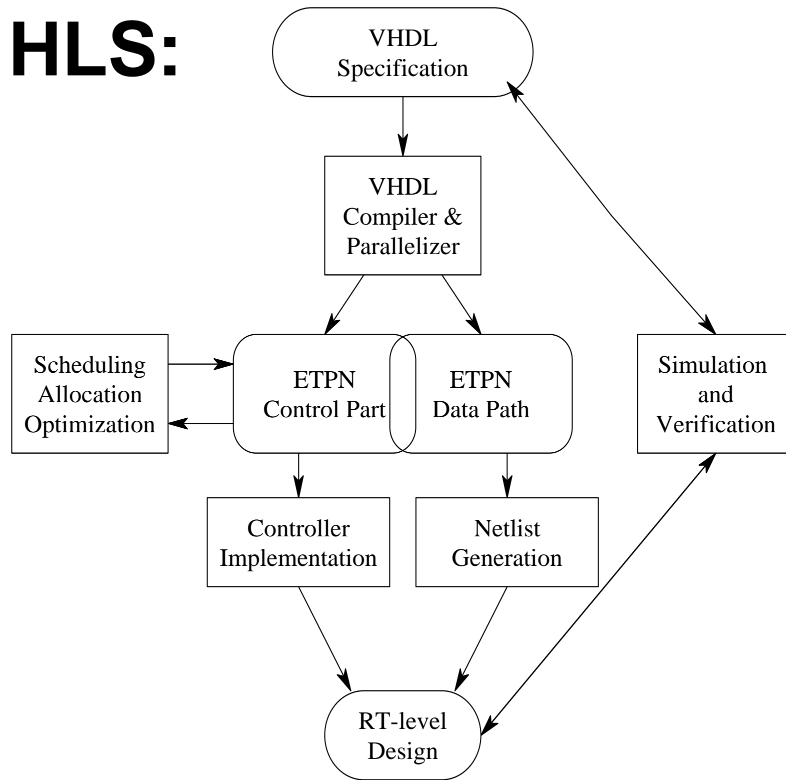
SP 3: Testability driven system design flow



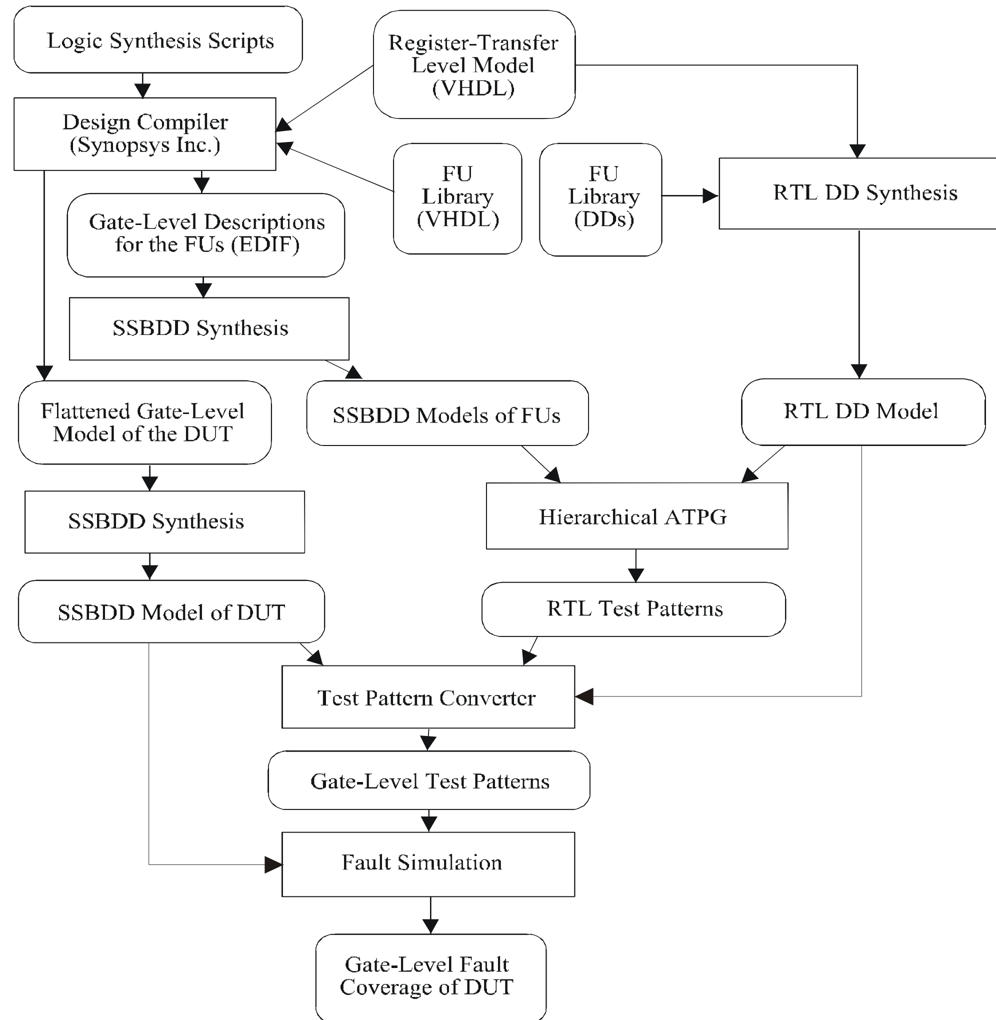
- **Combined**
  - **High-Level Synthesis system based on Extended Timed Petri Net representations, and**
  - **Hierarchical Test Pattern Generation, based on Decision Diagrams**
- **Interfaces to**
  - **behavioral and RT-level VHDL and**
  - **EDIF netlist formats**

SP 3: Testability driven system design flow

HLS:



TPG:



Subproject 4: Defect level test analysis

Subproject leader: **TTU**

Partners: **WUT, IIN , State University "Lvivska Politechnika, Ukraine**

Goals:

- **to carry out experiments of the quality of stuck-at tests to cover physical defects**
- **to create a hierarchical fault simulator for measuring the defect coverage**
- **to create a hierarchical test generator with high defect coverage**

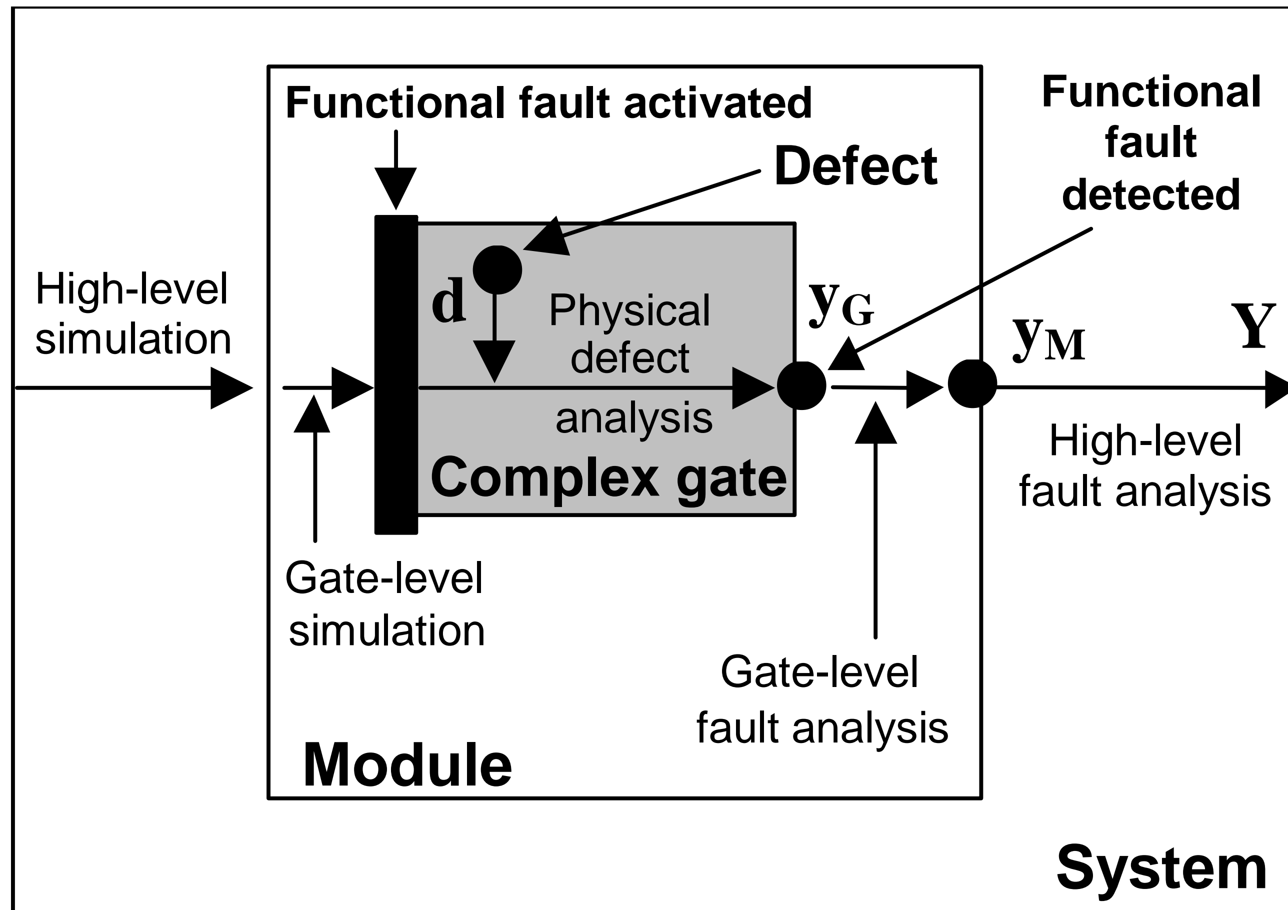
Roles of partners:

- **WUT, IIN: probabilistic defect analysis in CMOS gates**
- **TTU: gate- and RT-level fault simulation and test generation**

SP 4. Defect probabilities in a complex gate and a fault table

i	Fault d_i	Erroneous function f^{di}	p_i	Input patterns t_j															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	B/C	not((B*C)*(A+D))	0.010307065				1								1	1	1		
2	B/D	not((B*D)*(A+C))	0.000858922				1								1	1		1	
3	B/N9	B*(not(A))	0.043375564	1	1	1					1	1	1	1					
4	B/Q	B*(not(C*D))	0.007515568	1	1	1						1	1	1		1	1	1	
5	B/VDD	not(A+(C*D))	0.001717844									1	1	1					
6	B/VSS	not(C*D)	0.035645265													1	1	1	
7	A/C	not((A*C)*(B+D))	0.098990767				1				1					1	1		
8	A/D	not((A*D)*(B+C))	0.013098561				1				1					1		1	
9	A/N9	A*(not(B))	0.038651492	1	1	1		1	1	1					1				
10	A/Q	A*(not(C*D))	0.025982392	1	1	1		1	1	1						1	1	1	
11	A/VDD	not(B+(C*D))	0.000214731					1	1	1									
12	C/N9	not(A+B+D)+(C*(not((A*B)+D)))	0.020399399		1			1	1			1	1						
13	C/Q	C*(not(A*B))	0.033927421	1	1		1	1	1		1	1	1		1				
14	C/VSS	not(A*B)	0.005153532				1				1				1				
15	D/N9	not(A+B+C)+(D*(not((A*B)+C)))	0.007730298			1		1		1		1		1					
16	D/Q	D*(not(A*B))	0.149452437	1		1	1	1		1	1	1		1	1				
17	N9/Q	not((A*B)+(B*C*D)+(A*C*D))	0.143654713				1												
18	N9/VDD	not((C*D)+(A*B*D)+(A*B*C))	0.253382006													1			
19	Q/VDD	SA1 at Q	0.014386944				1				1				1	1	1	1	1
20	Q/VSS	SA0 at Q	0.095555078	1	1	1		1	1	1		1	1	1					

SP4: Hierarchical defect level test analysis



SP 4. Defect coverage for circuits C1, C2

Circuit	Probabilistic defect coverage, %		Denumerable defect coverage, %	
	T_{min}	T_{max}	T_{min}	T_{max}
C1	66,68	72,01	81,00	83,00
C2	70,99	77,05	84,29	84,76

Preliminary conclusions:

- **the difference between stuck-at fault and physical defect coverages reduces when the complexity of the circuit increases (C2 is more complex than C1)**
- **the difference between stuck-at fault and physical defect coverages is higher when the defect probabilities are taken into account compared to the traditional method where all faults are assumed to have the same probability.**

Conclusions

Results in the cooperative research:

- **Two ATPGs have been developed**
  - **hierarchical - for achieving very high speed, and**
  - **genetic - for achieving high fault coverage**
- **ATPGs have been integrated**
  - **into the FPGA design flow used in FhG EAS IIS Dresden, and**
  - **into the high-level synthesis (HLS) flow based on CAMAD HLS developed at Linköping University**
- **As the result of a wide international cooperation R&D work a novel hierarchical defect-oriented fault simulation method has been developed which allows to increase the quality of testing today's very large submicron integrated circuits**

Conclusions

- A Virtual Laboratory for cooperation in research, teaching and knowledge transfer in microelectronics design has been founded by 9 universities and research institutions from 6 European countries
- New research results in VL internationally recognized are already available
- New courses have been developed
- Links to industry are being created
- As the long-term effect of the project, new opportunities for cooperation associated with the VL will help to stabilize and increase the innovation potential in the CEE countries and strengthen the European position in the applications of IT