

Boundary-scan test for structural fault detection

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Outline

1. Introduction to the IEEE 1149.1 **Part 1**
boundary-scan test (BST) standard
2. The remote BST controller (MWS-TAP)

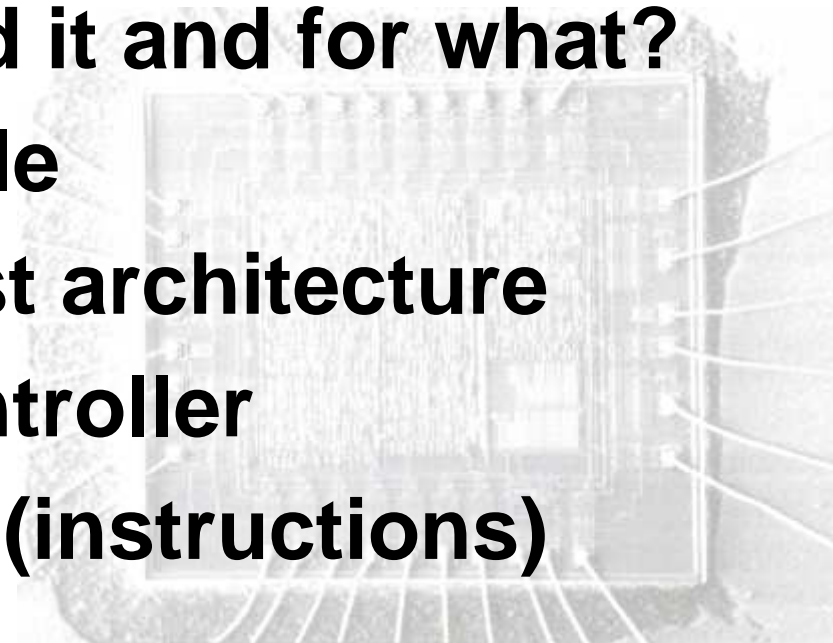
Break

3. The demonstration board
4. Open and short fault detection



1: The IEEE 1149.1 std (boundary-scan test)

- **Why do we need it and for what?**
- **The test principle**
- **BS cells and test architecture**
- **The on-chip controller**
- **The test modes (instructions)**

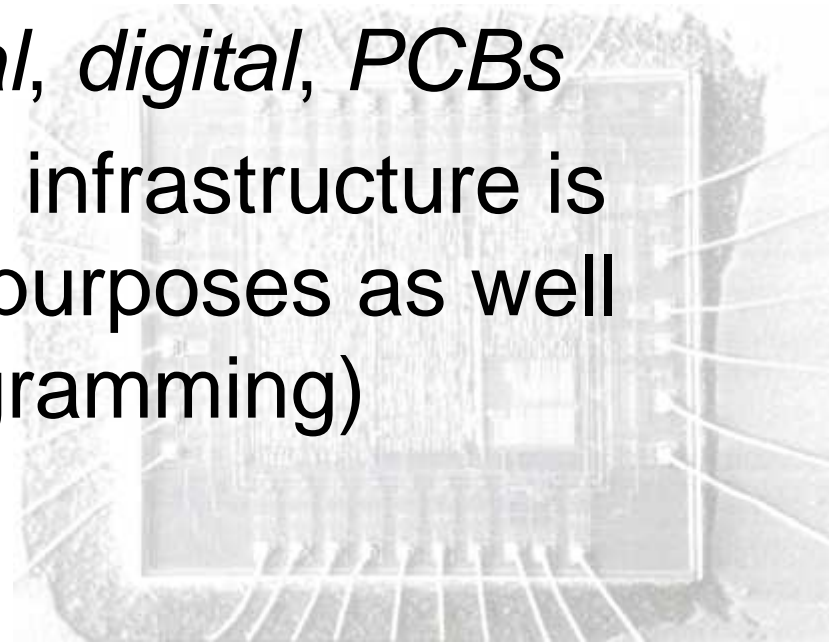


Why Boundary Scan Test?

- The two main reasons that led in the mid-80s to the development of BST were:
 - The complexity of ICs made it exceedingly difficult to develop test programs for the *functional test* of complex PCBs
 - Small outline surface mount devices and advanced mounting technologies almost disabled physical access to internal PCB nodes and made *in-circuit test* exceedingly difficult

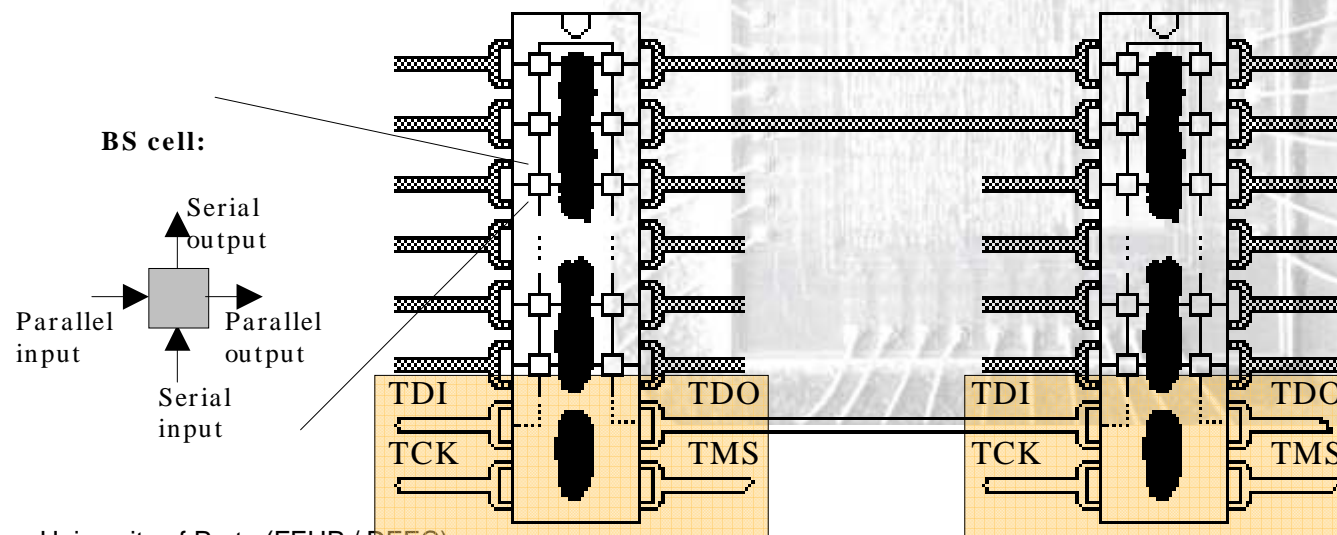
The application domain of BST

- BST addresses the structural test of digital printed circuit boards
- Keywords: *structural, digital, PCBs*
- This embedded test infrastructure is now used for other purposes as well (e.g. in-system programming)

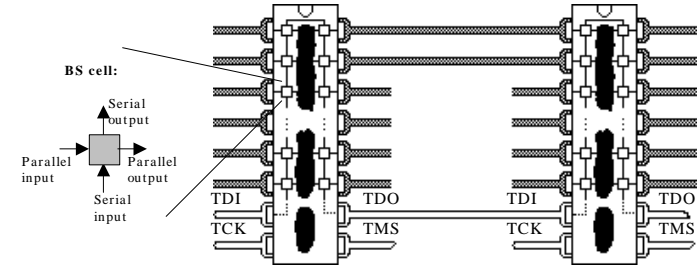


The BS test principle

- BS uses a *Test Access Port (TAP)* to decouple the internal IC logic from the pins and allows “direct” access to any PCB node without *backdriving* effects

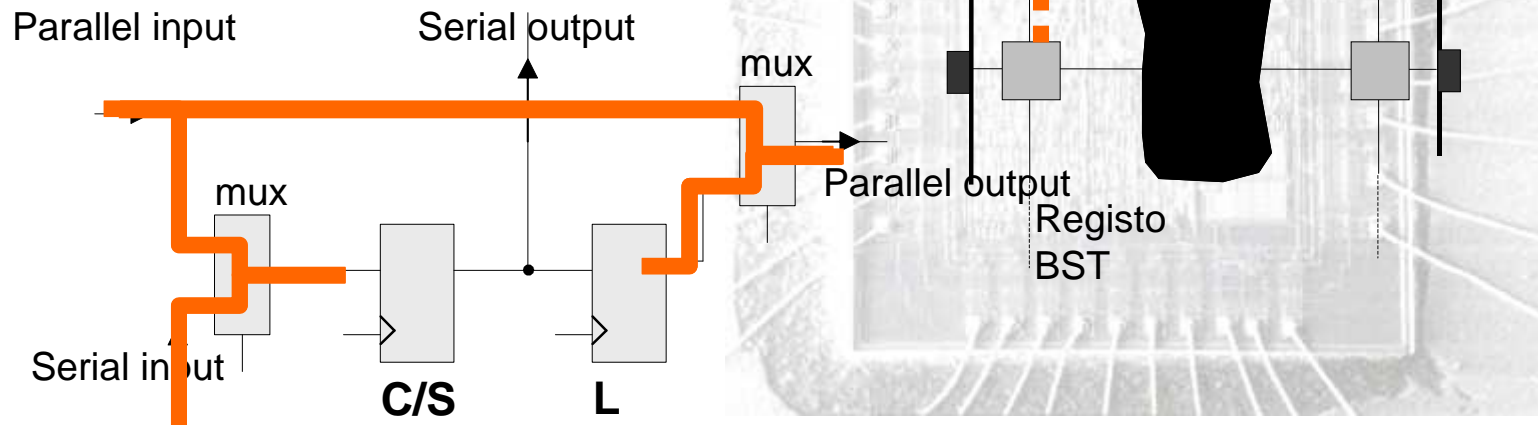


The basic BS cell



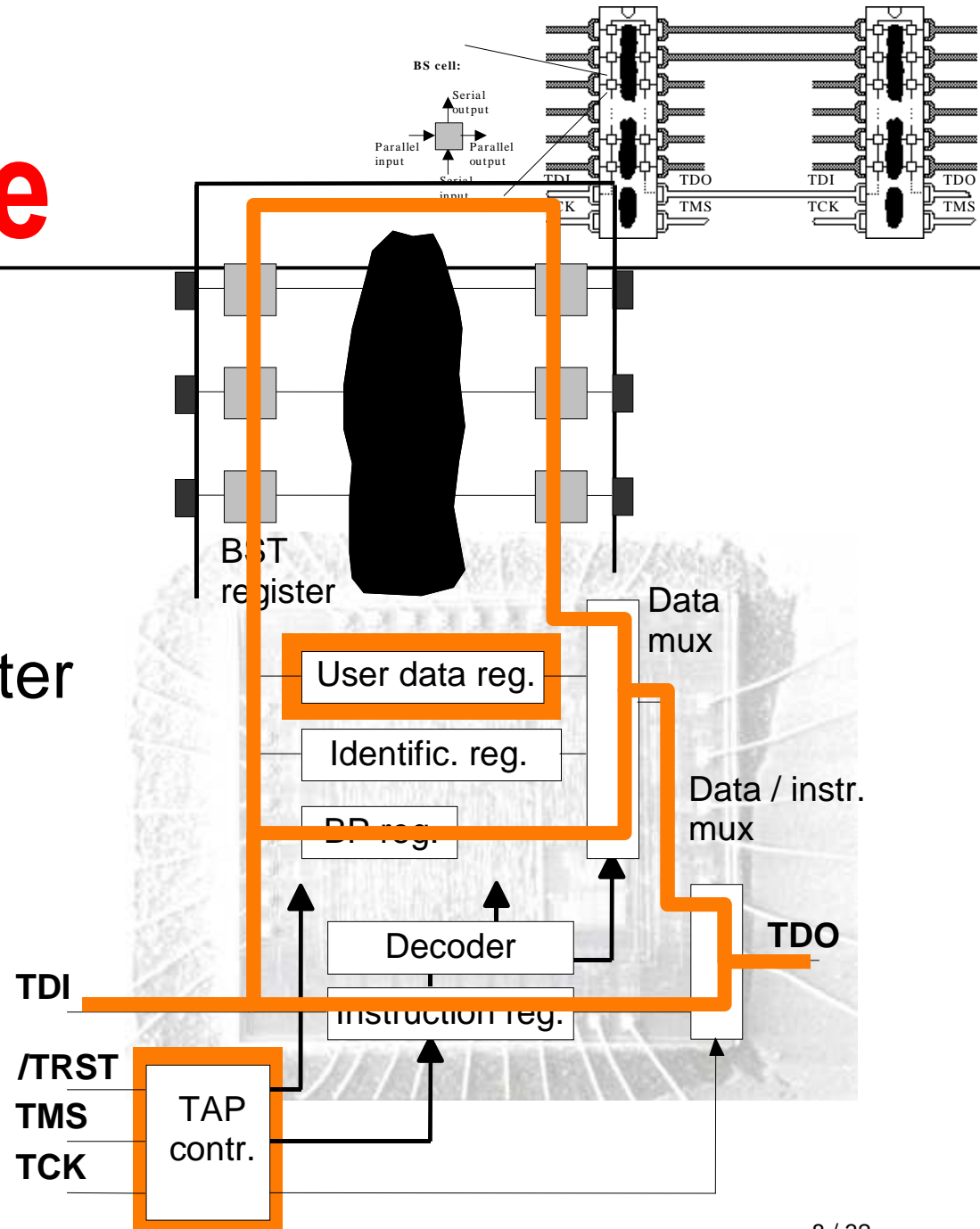
- Three modes of operation:

- ➔ Transparency
- ➔ Controllability
- ➔ Observability

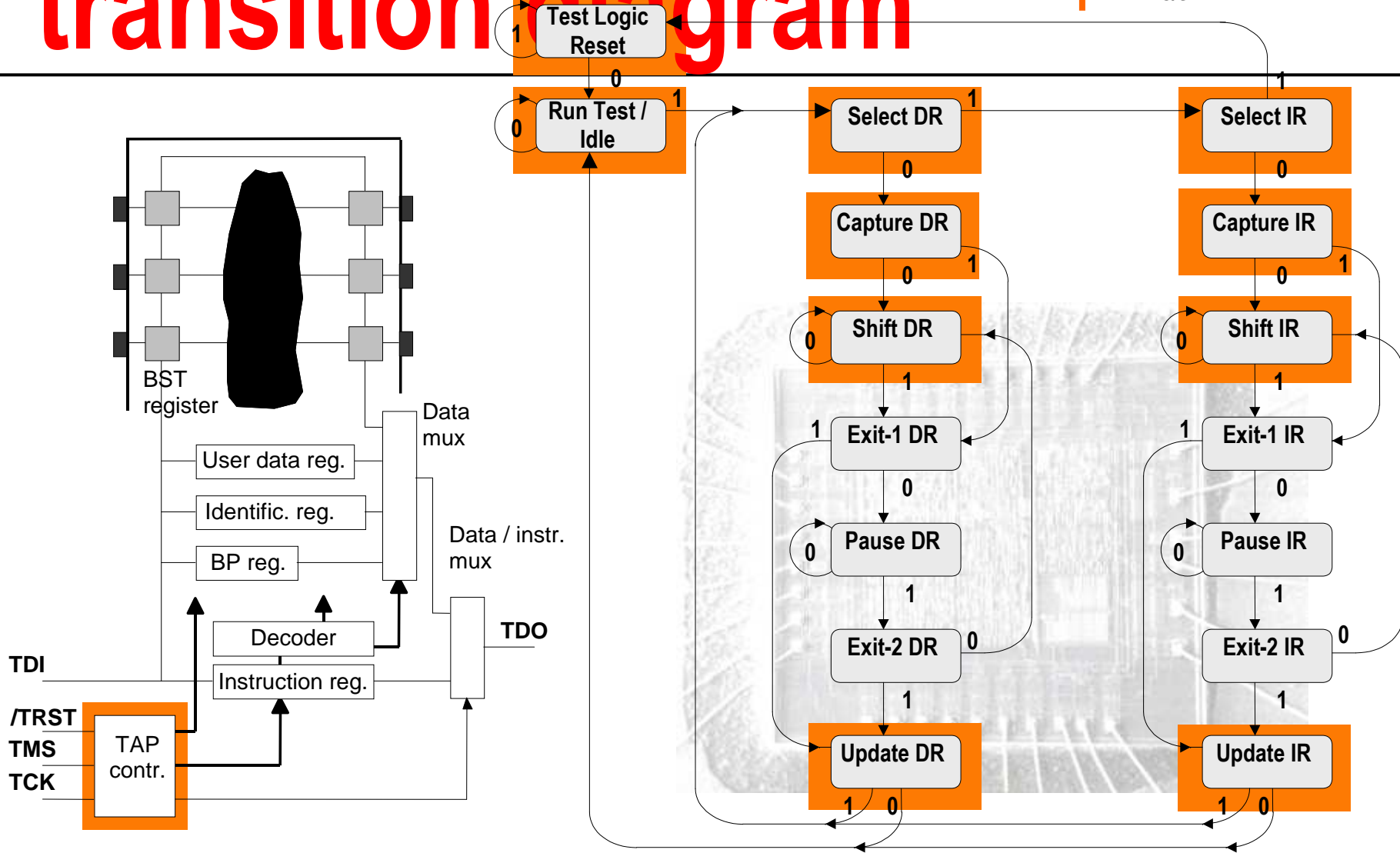
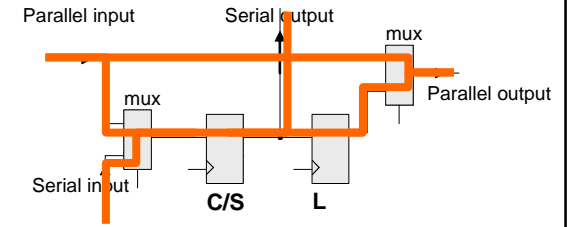


The BS architecture

- Main blocks:
 - ➔ BST register
 - ➔ BP register
 - ➔ Instruction register
 - ➔ TAP controller
 - ➔ Other registers

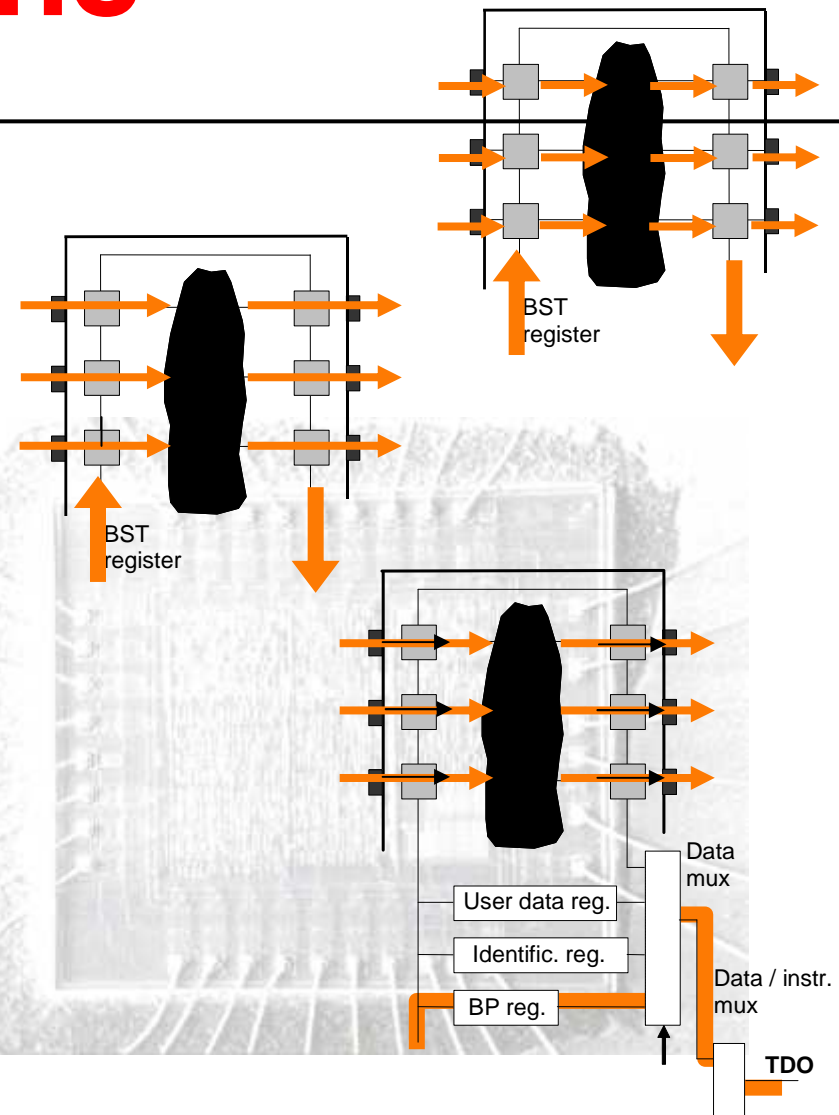


TAP controller state transition diagram



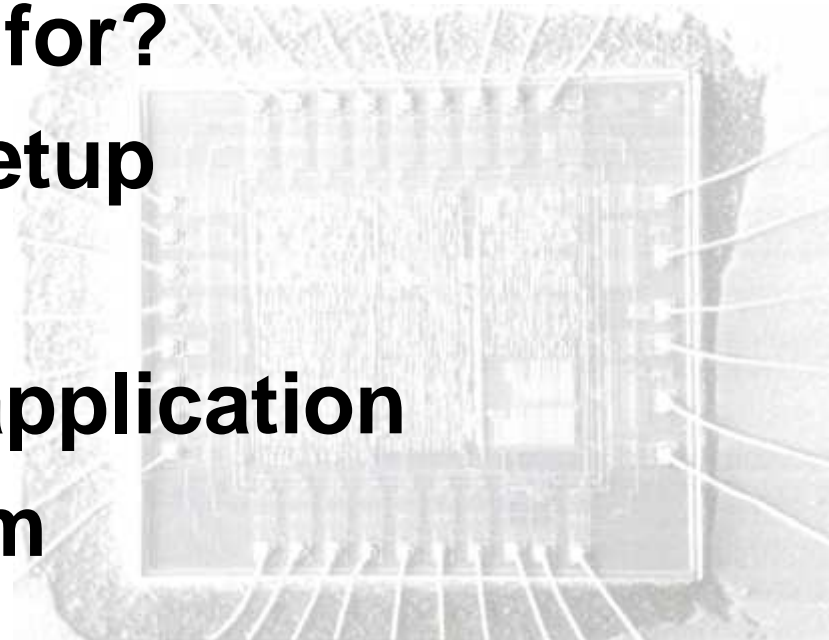
BST instructions

- Mandatory:
 - ➔ EXTEST
 - ➔ SAMPLE / PRELOAD
 - ➔ BYPASS
- Optional:
 - INTEST, RUNBIST, CLAMP, IDCODE, USERCODE, HIGHZ



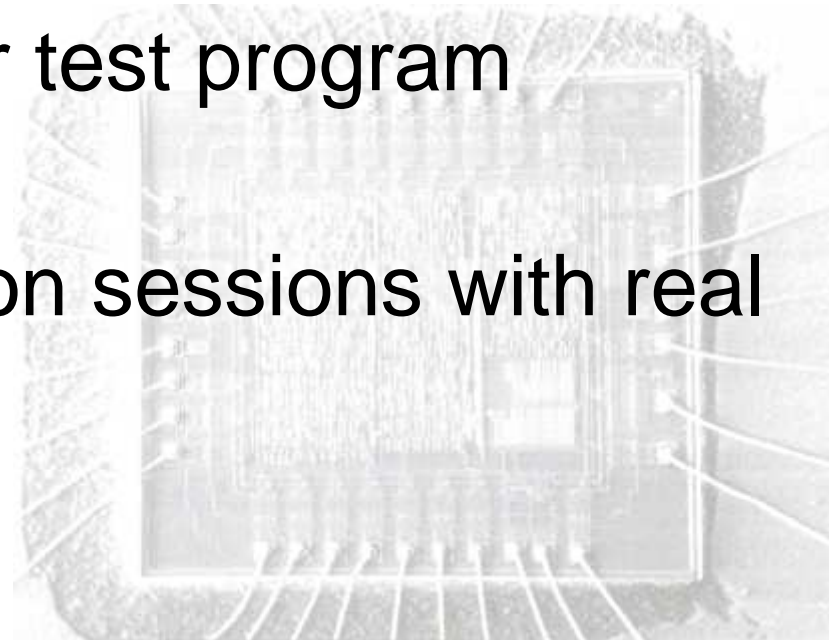
2: The remote BST controller (MWS-TAP)

- **Why / What is it for?**
- **The hardware setup**
- **Configuration**
- **The MWS-TAP application**
- **The test program**



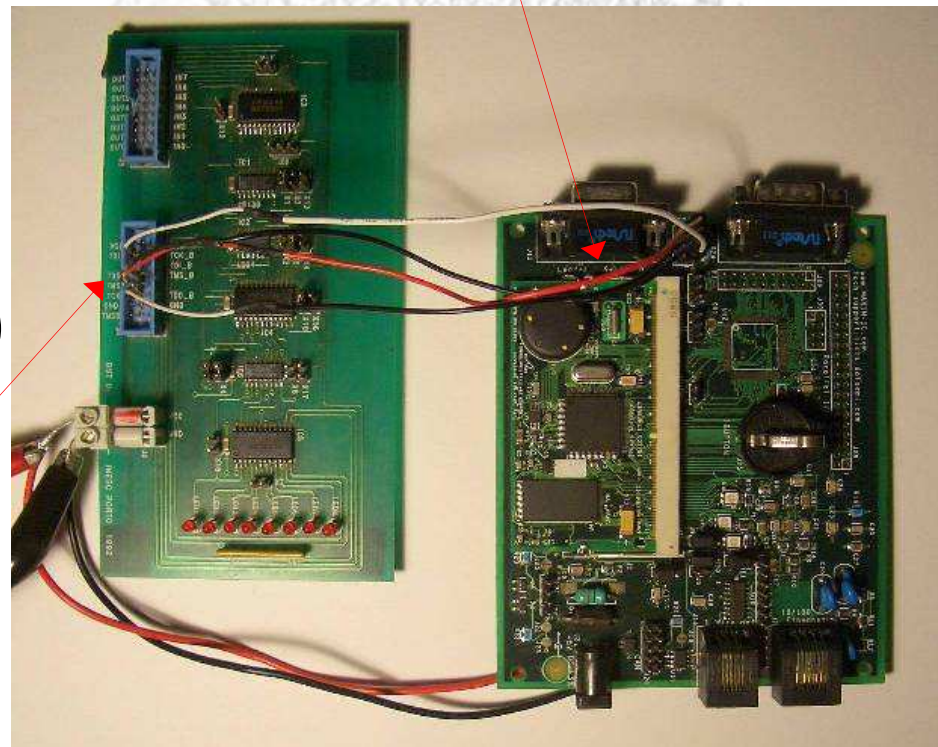
Why / what for?

- To enable the students to write real test programs in SVF and to execute online
- To provide a tool for test program validation
- To facilitate hands-on sessions with real 1149.X hardware

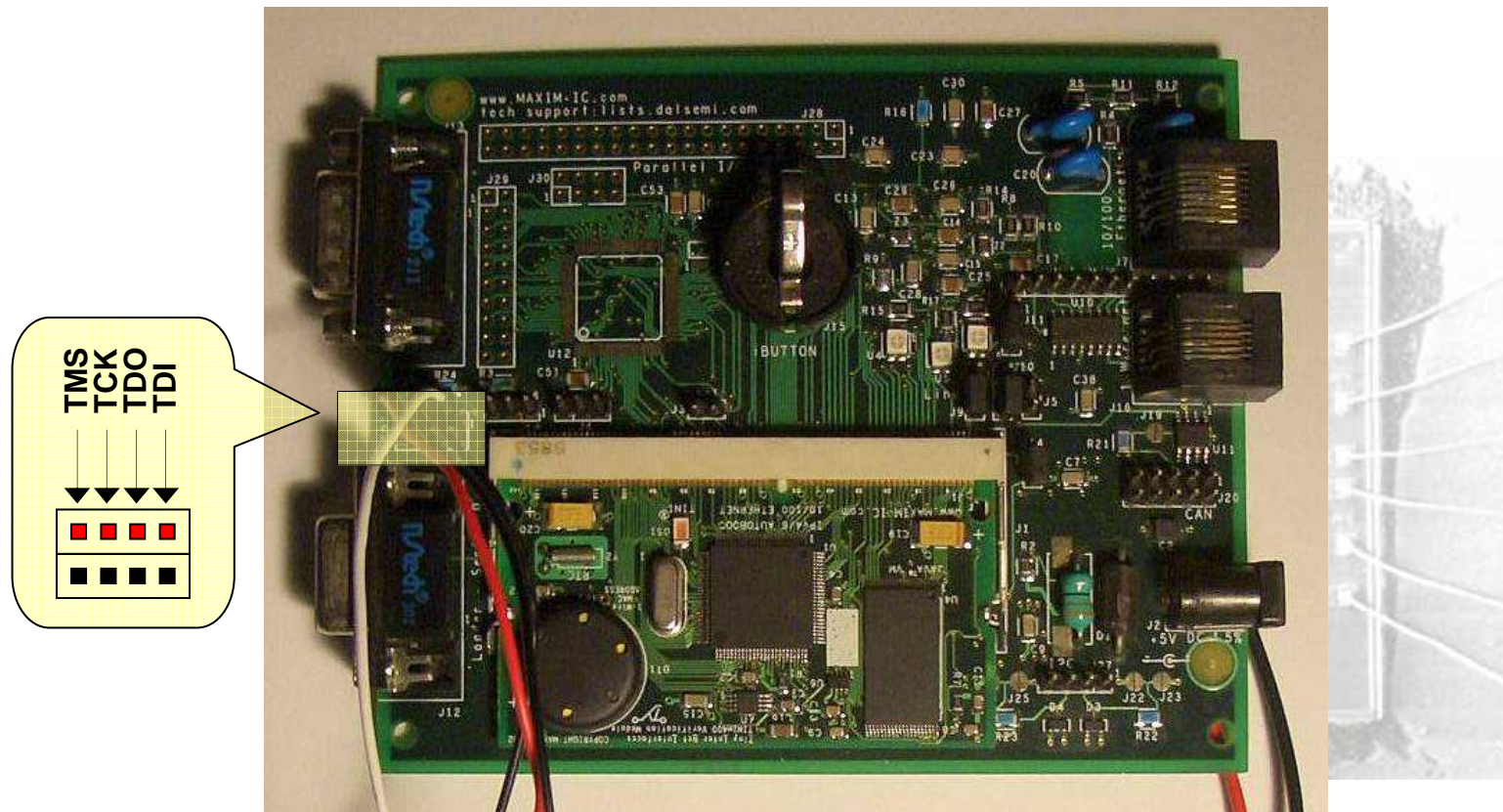


Setup: The MWS board

- The micro web server TAP controller application uses a **DSTINIm400** evaluation board (with a networked microcontroller from Maxim-Dallas)
- The current prototype controls **one BS chain**

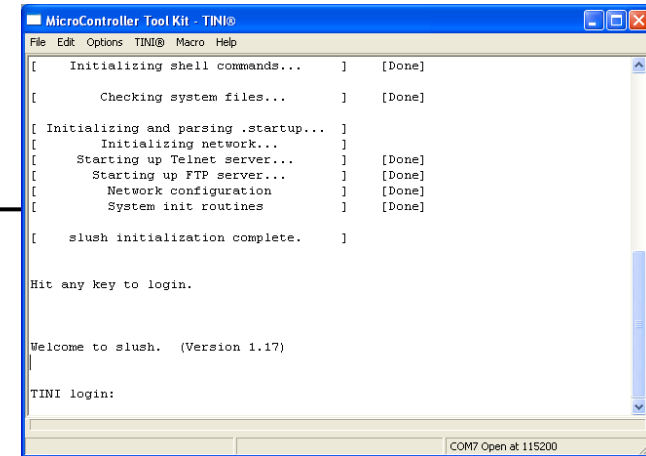


MWS board: the JTAG pins



Setup: IP and connections

- An RS232C port can be used to program a valid IP address into the micro web server board
- The server application can then be loaded by FTP and launched via Telnet

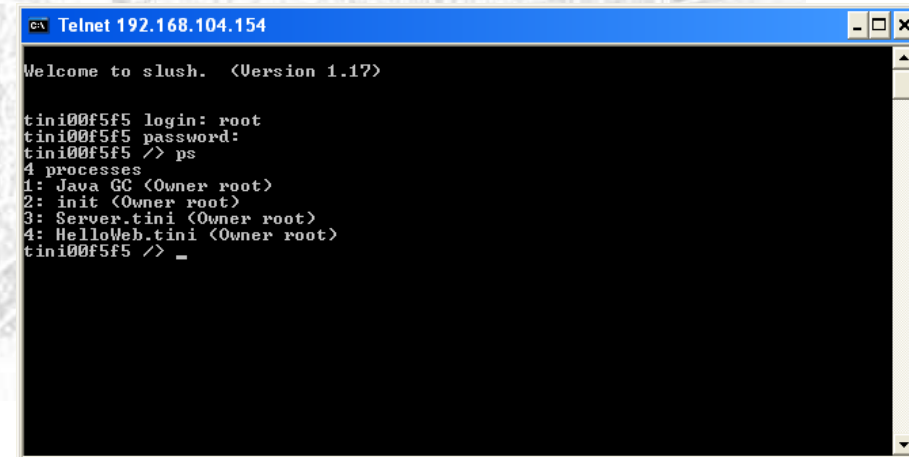


```
MicroController Tool Kit - TINI®
File Edit Options TINI® Macro Help
[ Initializing shell commands... ] [Done]
[ Checking system files... ] [Done]
[ Initializing and parsing .startup... ]
[ Initializing network... ]
[ Starting up Telnet server... ] [Done]
[ Starting up FTP server... ] [Done]
[ Network configuration ] [Done]
[ System init routines ] [Done]
[ slush initialization complete. ]

Hit any key to login.

Welcome to slush. (Version 1.17)

TINI login:
COM7 Open at 115200
```



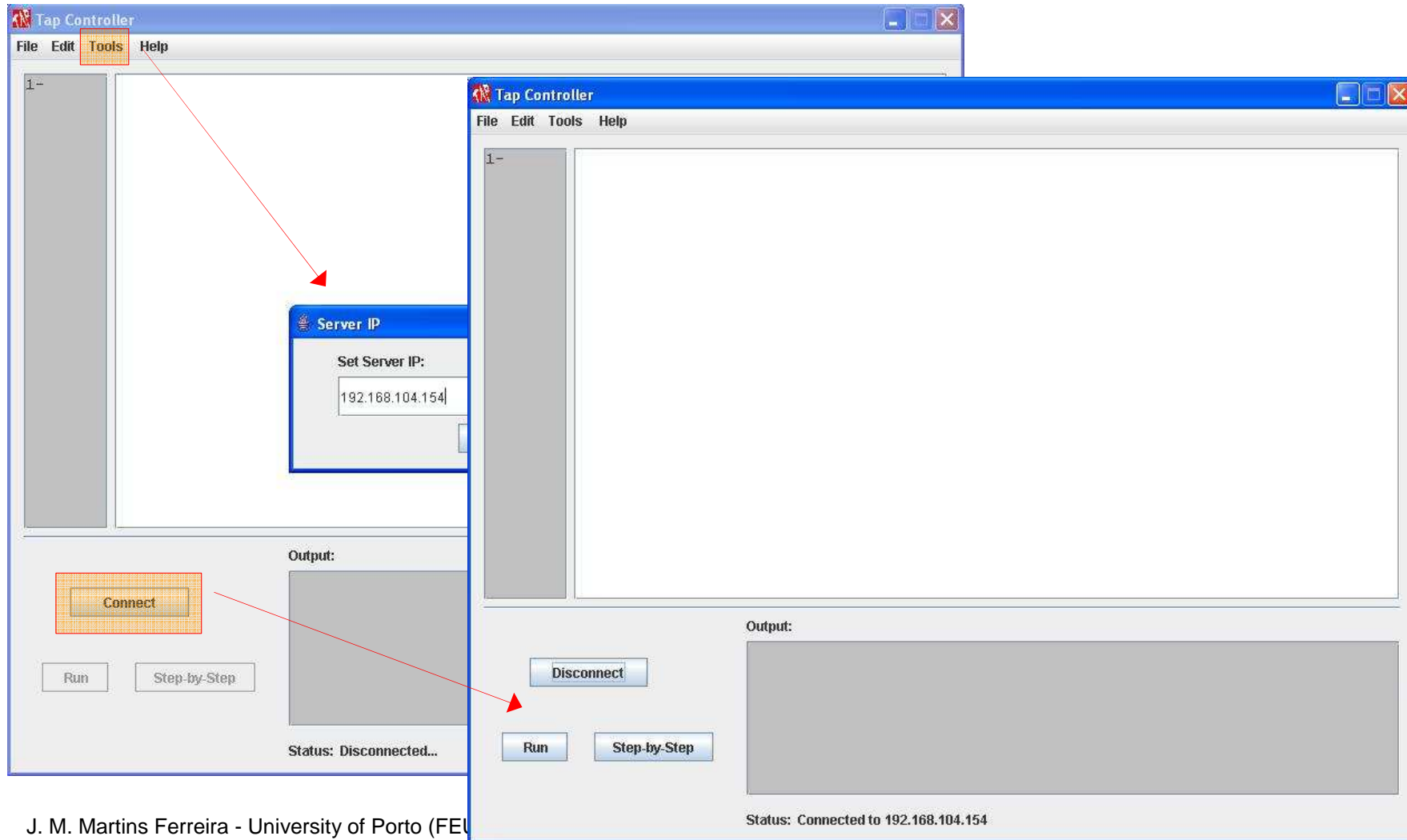
```
CA Telnet 192.168.104.154
Welcome to slush. <Version 1.17>

tini00f5f5 login: root
tini00f5f5 password:
tini00f5f5 /> ps
4 processes
1: Java GC <Owner root>
2: init <Owner root>
3: Server.tini <Owner root>
4: HelloWeb.tini <Owner root>
tini00f5f5 /> _
```

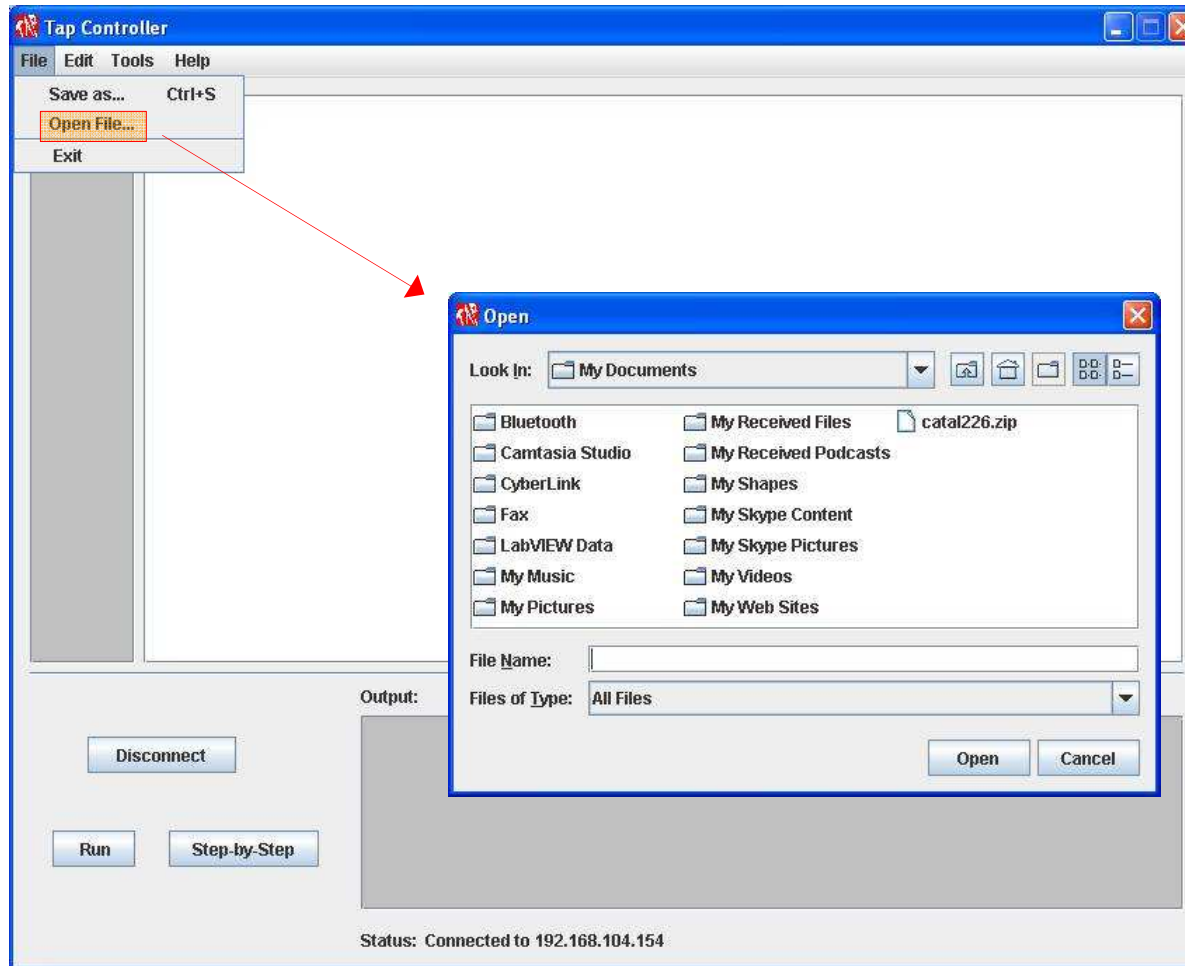
Set up (cont.)

- If the current IP of the MWS is known, a quicker set up procedure is possible:
 - Connect the card directly to a computer using a regular LAN cable and telnet to its IP address
 - Set up the new IP address (cuts the current connection if in different subnets),
e.g. `ipconfig -a 158.36.164.12 -m 255.255.254.0 -g 158.36.164.1`
 - Set the current IP of the computer to the same subnet and reconnect (or use the LAN)

MWS-TAP – set IP address and connect



MWS-TAP – Open / write a new SVF test program



Boundary-scan test for structural fault detection

Short break!



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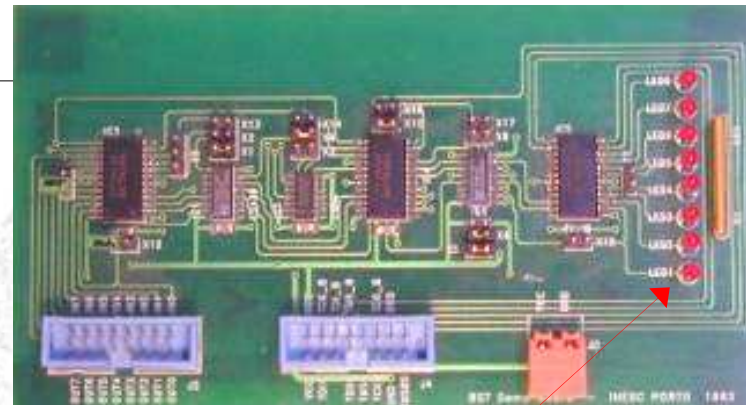
Break

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4. Open and short fault detection

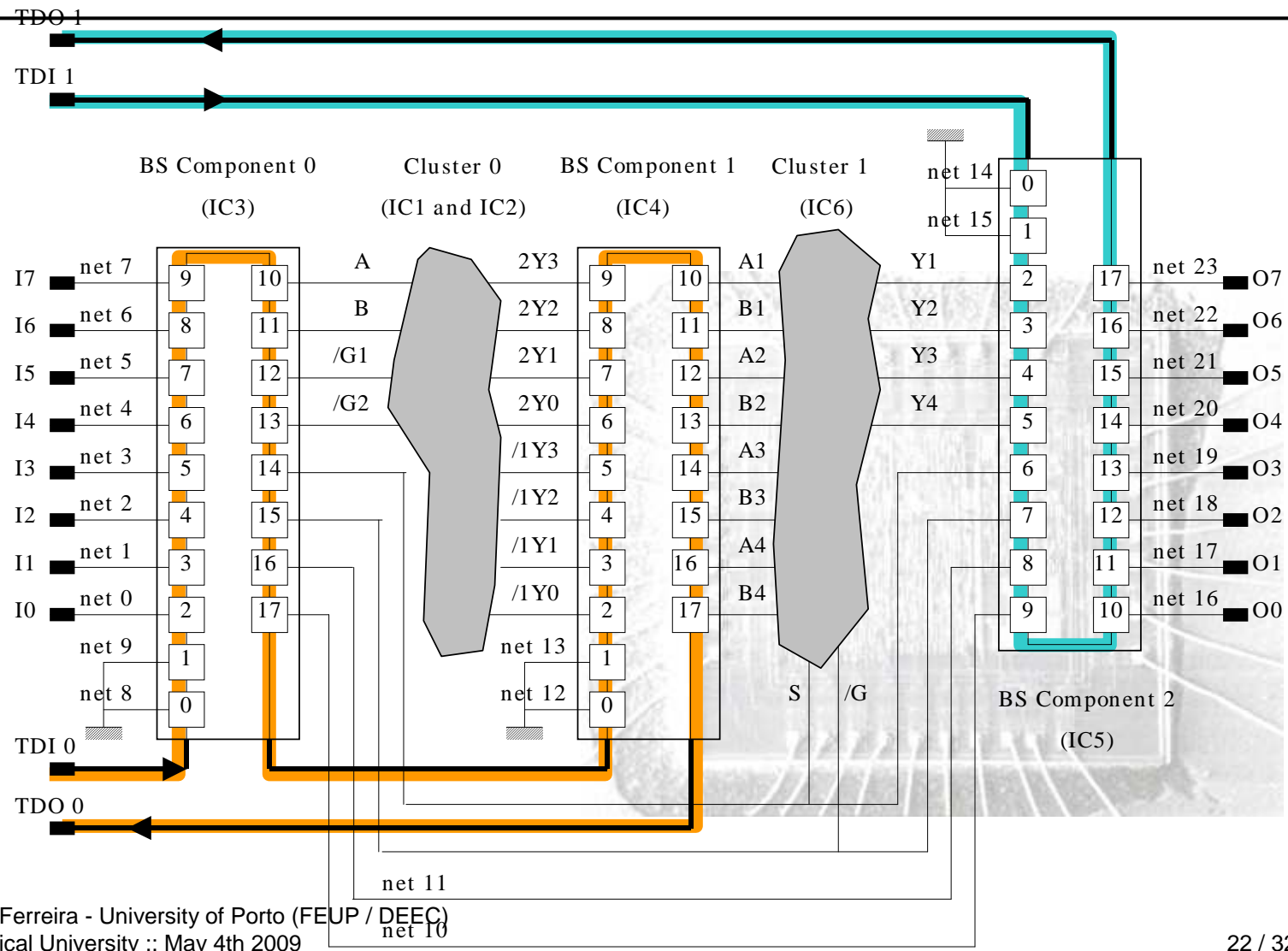
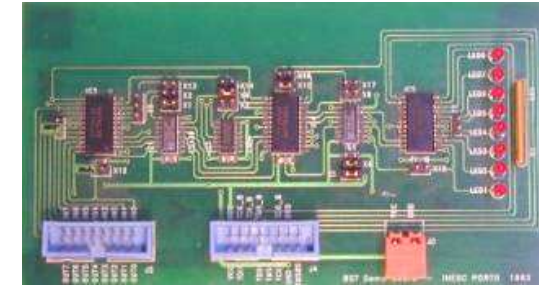
Part 2

3: The demonstration board

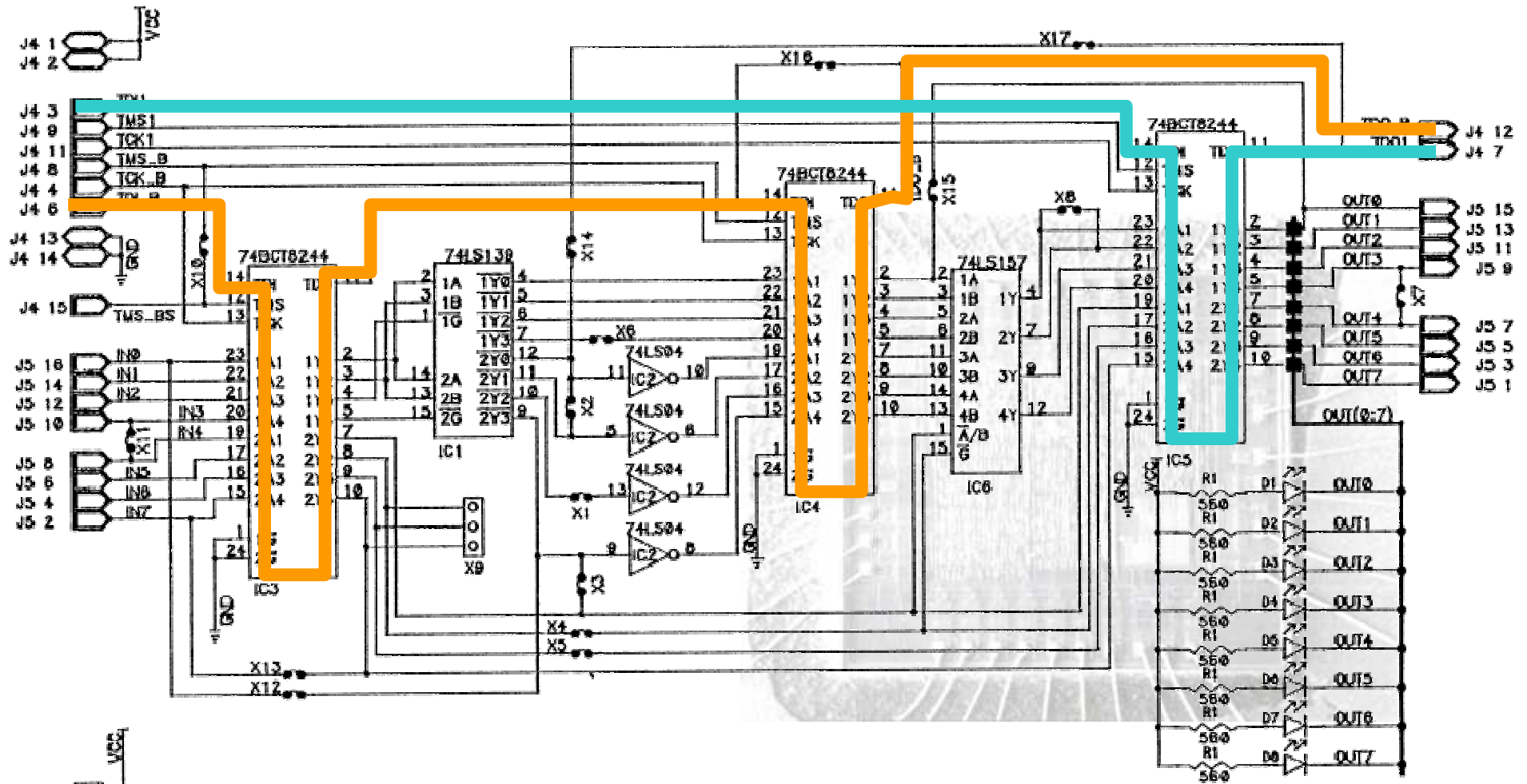
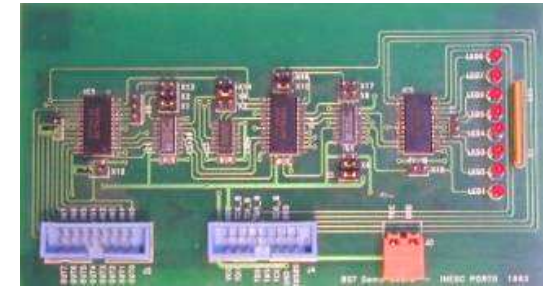
- What's in it?
- Schematic
- Integrity check
- BS in practice (led control)



Block diagram of the demonstration board

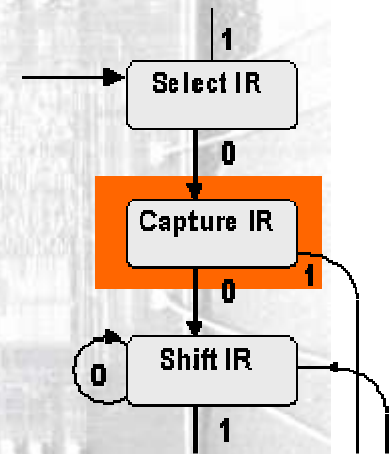
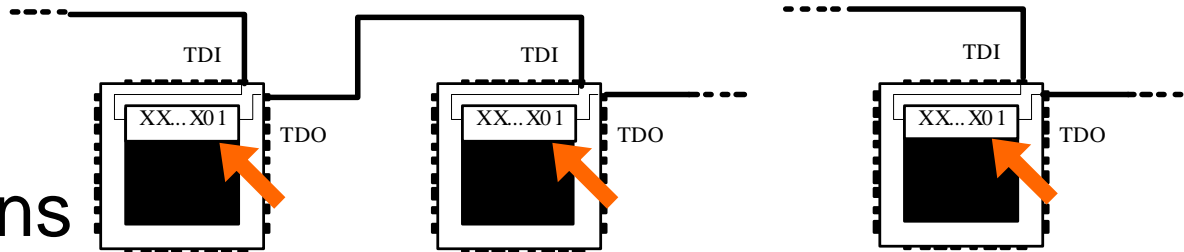


Schematic diagram



Integrity check of the BS infrastructure

- Detection of:
 - Faulty TAP pins
 - Faulty / misplaced components
- Sequence of operations:
 - Reset (TRST or 5 x TMS1)
 - IR capture and scan
 - ID capture and scan (if supported)



Led control

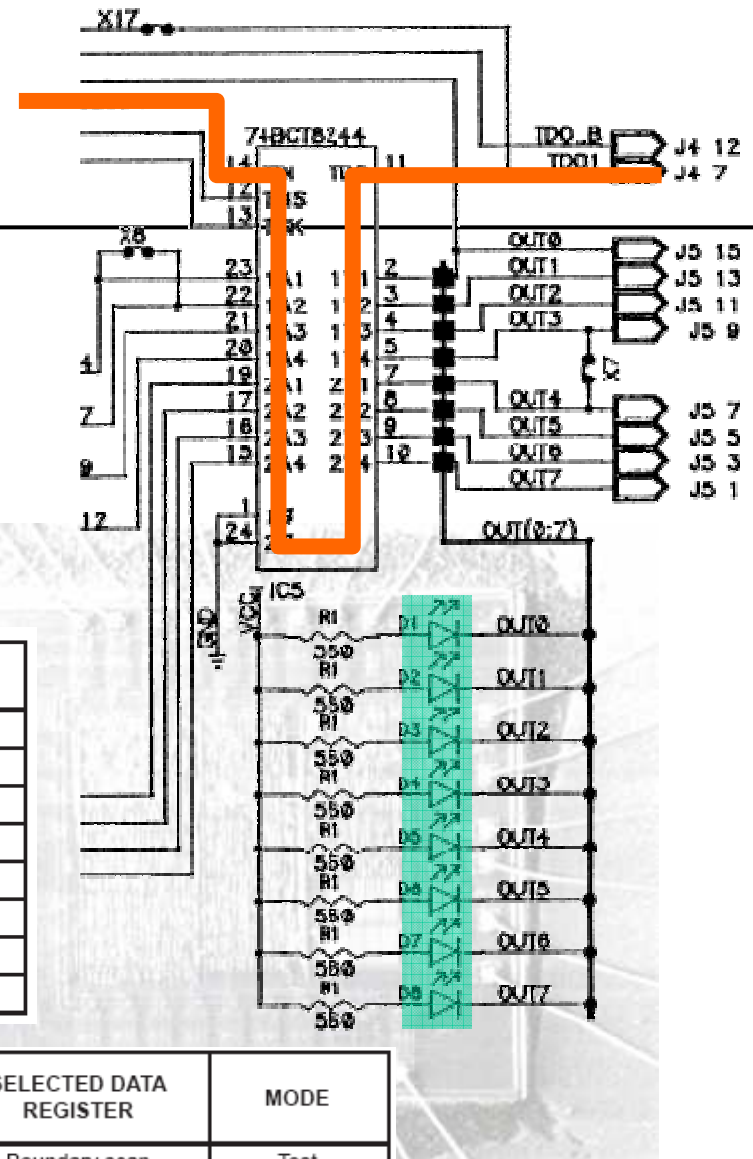
- What BS instruction?
- What test vector (into the BS register)?

BS register

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
17	1OE	15	1A1	7	1Y1
16	2OE	14	1A2	6	1Y2
-	-	13	1A3	5	1Y3
-	-	12	1A4	4	1Y4
-	-	11	2A1	3	2Y1
-	-	10	2A2	2	2Y2
-	-	9	2A3	1	2Y3
-	-	8	2A4	0	2Y4

instructions

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
X0000000	EXTTEST/INTEST	Boundary scan	Boundary scan	Test
X0000001	BYPASS‡	Bypass scan	Bypass	Normal
X0000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal



MWS-TAP – Example (led control)

The image displays two screenshots of the Tap Controller software interface, showing the execution of an SVF file. The left screenshot shows the initial state of the software, with the SVF code loaded and the 'Run' button highlighted. The right screenshot shows the software after execution, with the 'Output' window displaying the results of the test.

Left Screenshot: Tap Controller - demo-leds.svf

```
1- ! This SVF code controls the leds...
2- ! ... in the BS demonstration board
3- STATE RESET
4- ! The next command shifts in the EX
5- ! ... and does an infrastructure te
6- SIR 8 TDI(00) TDO(81) MASK(FP)
7- ! We now scan the data vector to th
8- SDR 18 TDI(00055)
```

Buttons: Disconnect, Run, Step-by-Step

Status: Connected to 192.168.104.154

Right Screenshot: Tap Controller - demo-leds.svf

```
1- ! This SVF code controls the leds...
2- ! ... in the BS demonstration board
3- STATE RESET
4- ! The next command shifts in the EXTEST code...
5- ! ... and does an infrastructure test
6- SIR 8 TDI(00) TDO(81) MASK(FP)
7- ! We now scan the data vector to the leds
8- --> SDR 18 TDI(00055)
```

Buttons: Disconnect, Run, Step-by-Step

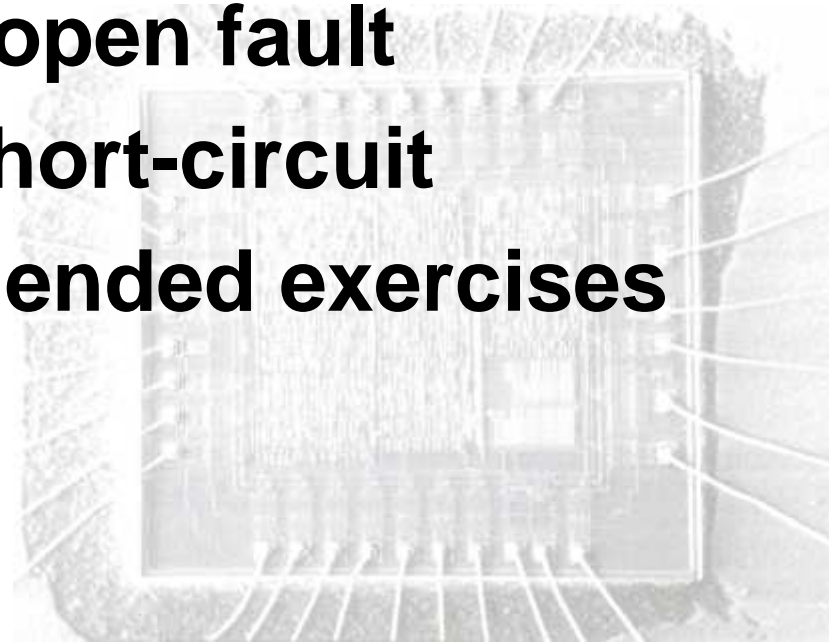
Output:

```
Line6:
Present State: RESET
Visited states: IDLE DRSELECT IRSELECT RESET
Line6:
String shifted out: 0x81
Scan error: NO ERROR DETECTED!
Present State: IDLE
Visited states: RESET IDLE DRSELECT IRSELECT IRCAPTURE IRSHIFT IREXIT1 IRUPDATE IDLE
```

Status: Connected to 192.168.104.154

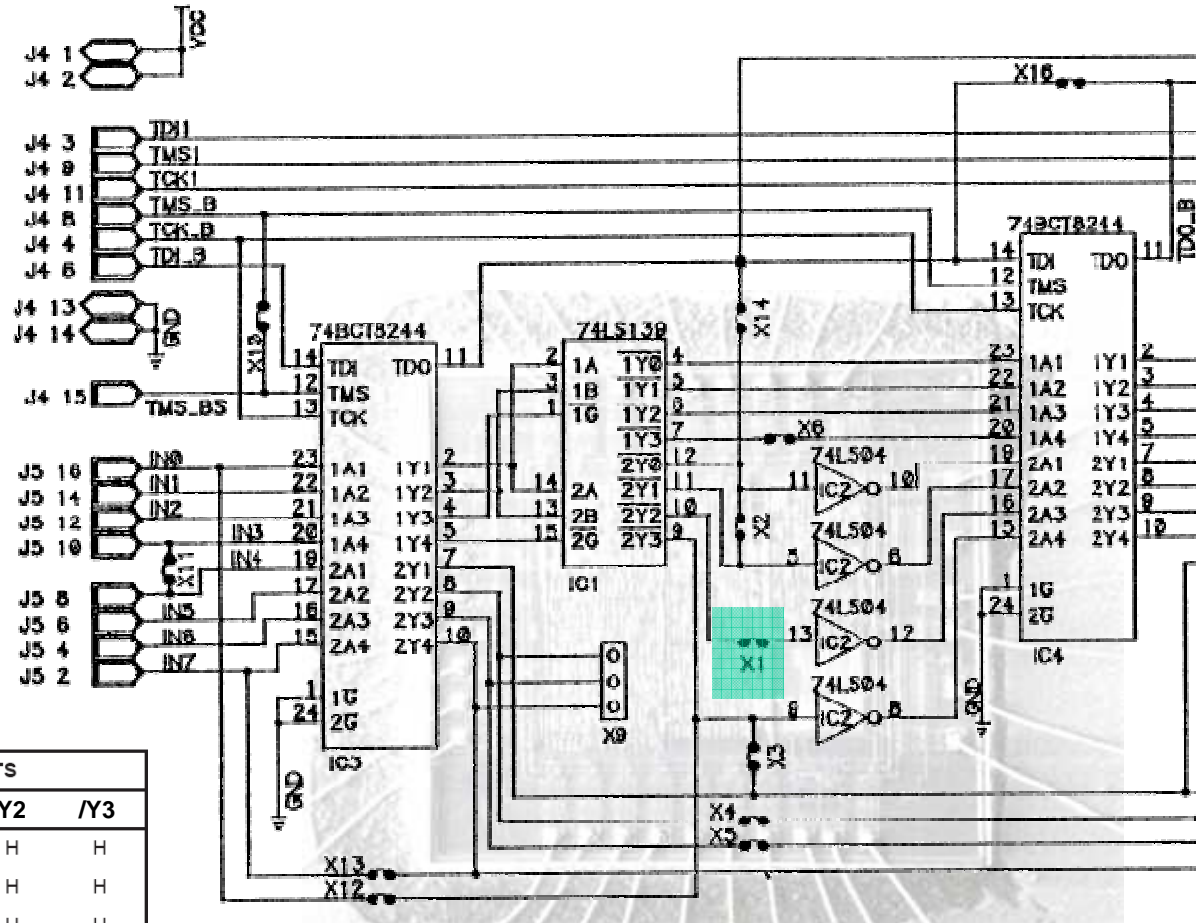
4: Open and short fault detection

- **Detection of an open fault**
- **Detection of a short-circuit**
- **Further recommended exercises**



Detection of open circuit X1

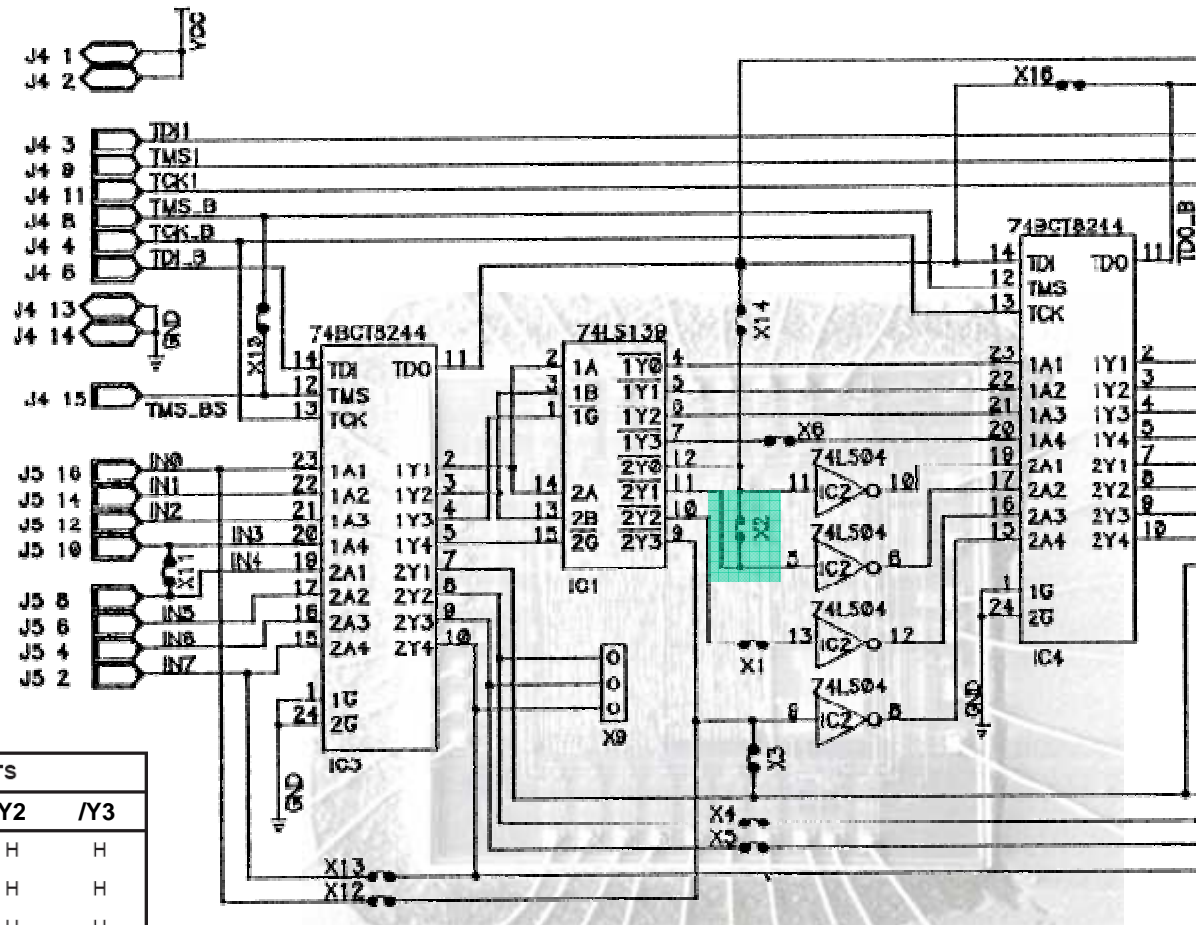
- What conditions enable the detection of open circuit X1?



INPUTS			OUTPUTS			
/G	A	B	/Y0	/Y1	/Y2	/Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

Detection of short-circuit X2

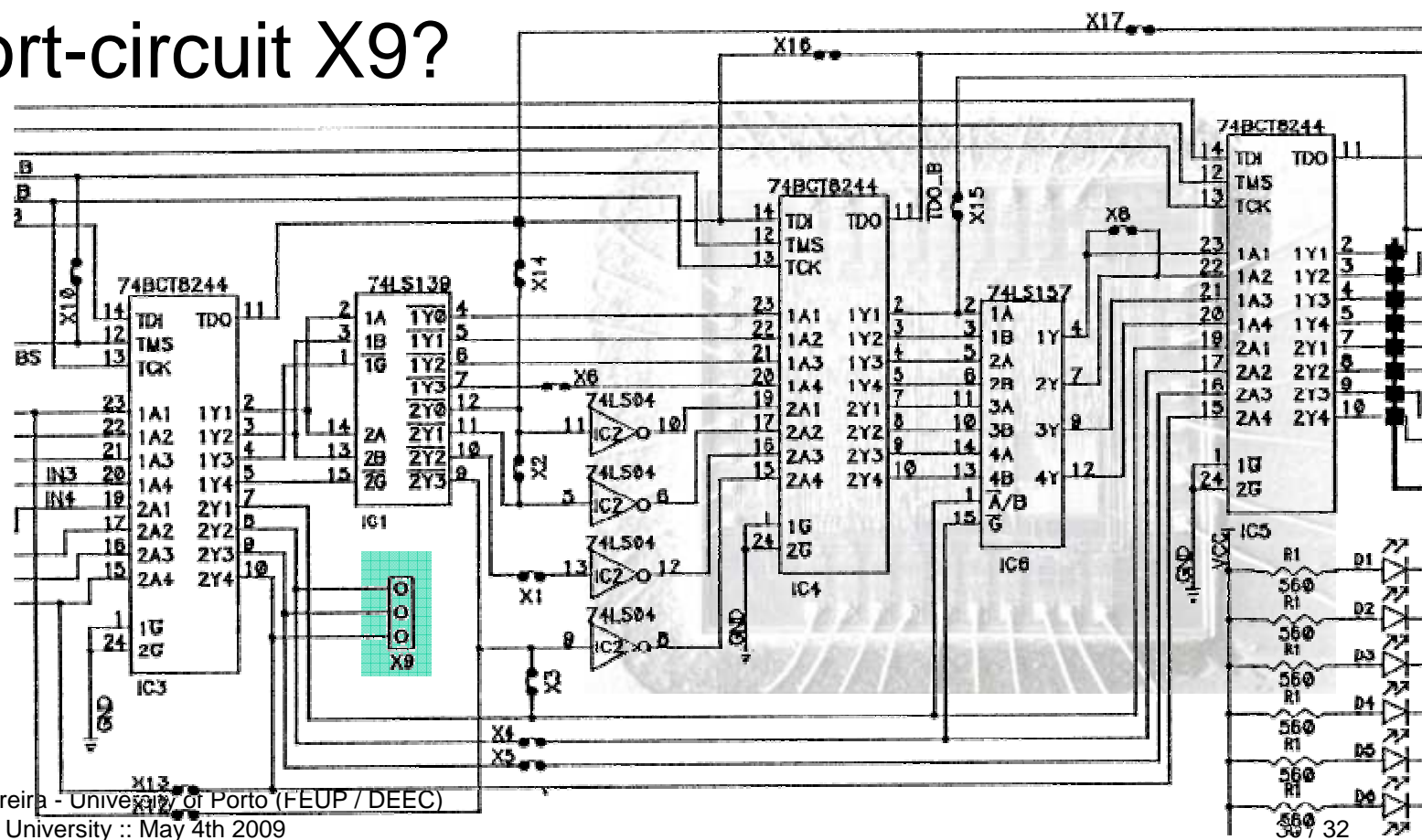
- What conditions enable the detection of short circuit X2?



INPUTS			OUTPUTS			
/G	A	B	/Y0	/Y1	/Y2	/Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

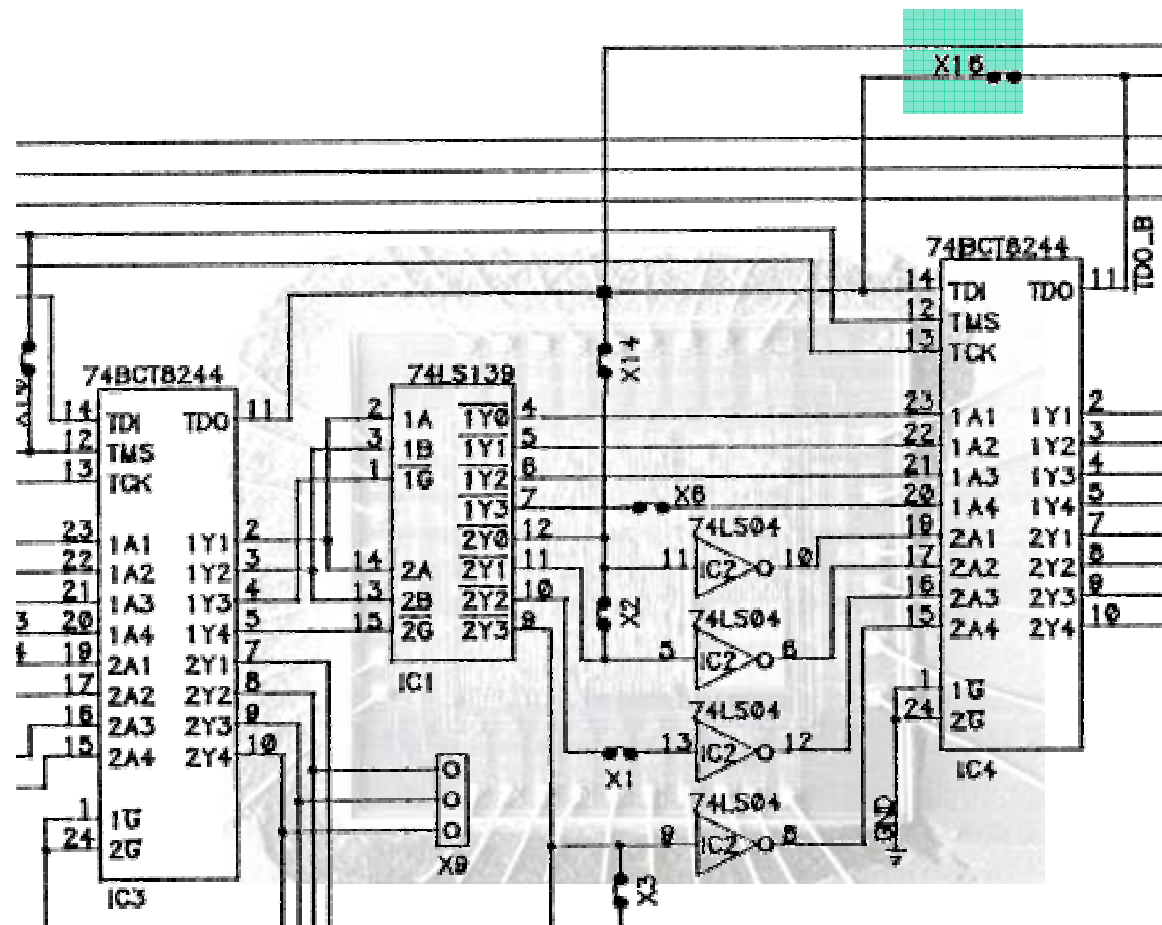
Detection of short circuit X9

- What conditions enable the detection of short-circuit X9?



Detection of short circuit X16

- What conditions enable the detection of short-circuit X16?



Boundary-scan test for structural fault detection

Thanks for your attention!

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