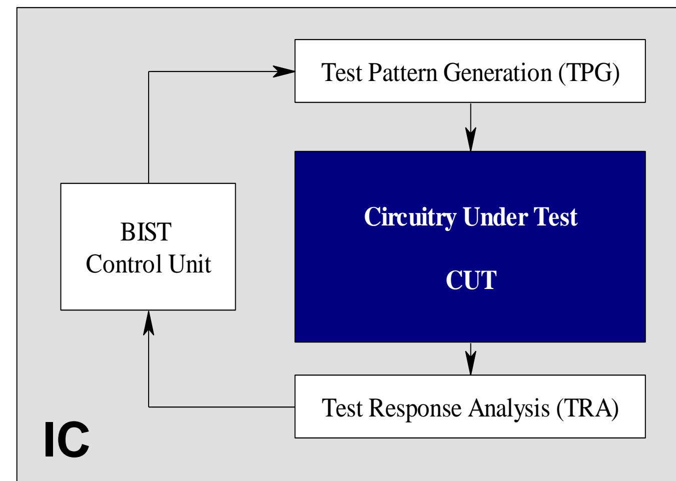
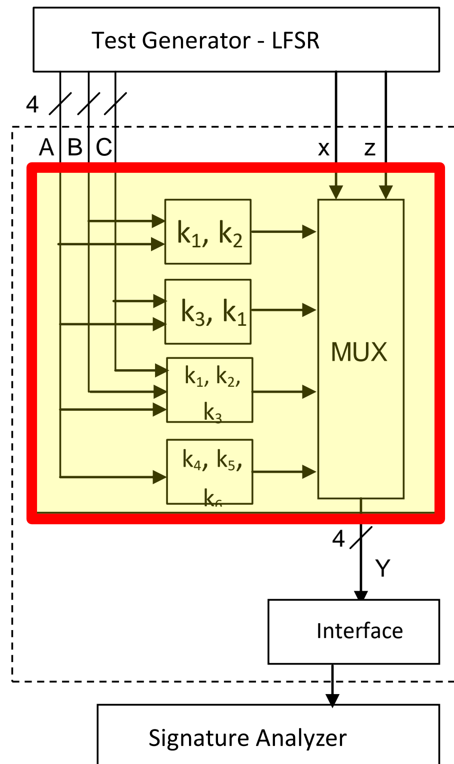
Course Work (Simplified): Built-In Self-Test

Problems:

- **BIST modeling and simulation**
  - **Test pattern generation** (quality?, test length?)
  - **Response verification**
- **Pseudorandom test**
  - very long tests?
- **Hybrid test solutions**
- **Response compression**



Course Work: Research Object



1. Design of a combinational circuit for the following functionality

If x = 0, z = 0, then $Y = k_1A + k_2B$, else

if x = 0, z = 1, then $Y = k_3A - k_1C$, else

if x = 1, z = 0, then

$Y = (k_1A \vee k_1B \wedge k_2C) \oplus (k_3C \vee \text{NOT}(k_3A) \wedge k_1B)$,

else

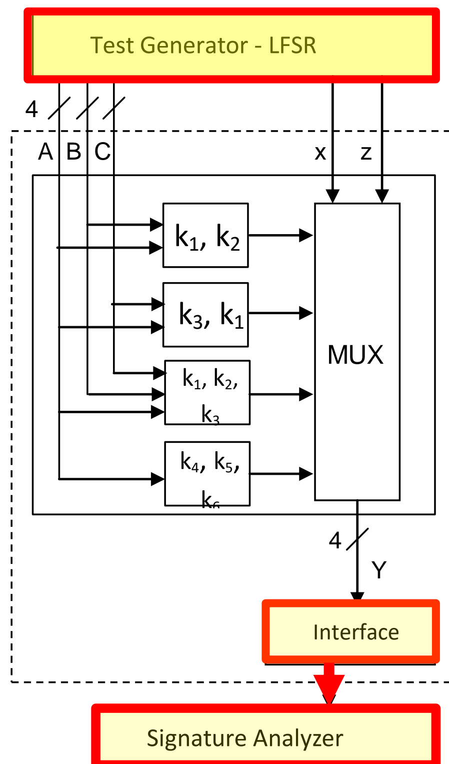
if x = 1, z = 1, then $Y = k_4A^2 + k_5A + k_6$

Coefficients k_i can be found on the next slide

Course Work: Versions of Research Object

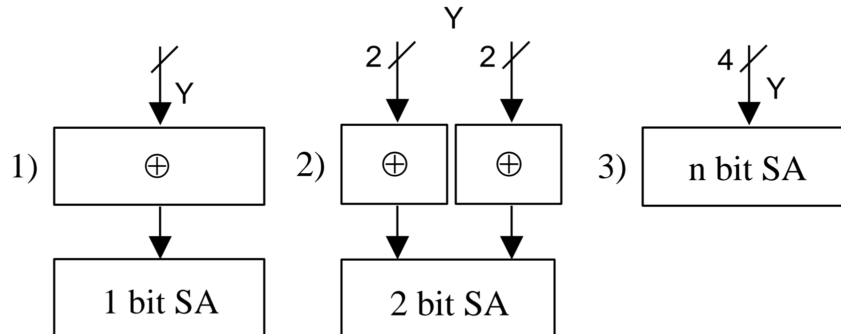
Vers. No.	k_1	k_2	k_3	k_4	k_5	k_6	Vers no.	k_1	k_2	k_3	k_4	k_5	k_6
1	1	1	1	0,1	0,2	0,5	8	1	1	1	1,5	0,1	0,5
2	1	1	0	0,1	0,2	1,0	9	1	1	0	1,5	0,1	1,0
3	1	0	1	0,1	0,2	2,0	10	1	0	1	1,5	0,4	2,0
4	1	0	0	0,1	0,2	3,0	11	1	0	0	1,5	0,4	3,0
5	0	1	1	0,1	1,0	0,5	12	0	1	1	1,5	0,8	0,5
6	0	1	0	0,1	1,0	1,0	13	0	1	0	1,5	0,8	1,0
7	0	0	1	0,1	2,0	2,0	14	0	0	1	1,5	1,5	2,0
15	1	1	1	0,2	0,4	1,0	20	0	0	1	0,5	0,4	1,0
16	1	1	1	0,1	0,4	1,2	21	0	0	1	1,0	0,8	1,5
17	1	1	0	0,2	0,4	0,5	22	0	1	1	0,5	1,2	0,5
18	1	0	1	0,2	0,4	1,0	23	0	1	1	1,0	0,3	1,0
19	0	0	1	0,3	2,0	1,0	24	1	0	1	0,4	1,0	1,5

Course Work: Design of Interface



2. Design of the experimental bench. Use three different interface versions for experiments: 1 bit, 2-bit and 4- or more bit interfaces for respective n-bit Signature Analyzers

The types of interface:

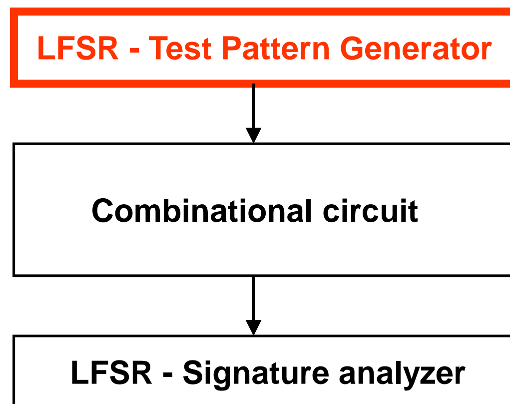


Course Work: Design of a Testable Circuit

3. Enter the designed gate-level (AND, OR, NOT) circuit into the computer by CADENCE circuit editor
4. Testability analysis. Generate test patterns with Turbo-Tester (TT) ATPG to achieve the fault coverage as close to 100% as possible

Course Work: Design of a Test Generator

BILBO - Built- In Logic Block Observer:



7. Generate test patterns by the BILBO tool for 10 different polynomials, and find the best structure for the LFSR

   Choose 5 primitive, and 5 non-primitive polynomials

   Report for all 10 experiments

   a) the maximum achievable fault coverage, and

   b) fix the minimum test length needed for that

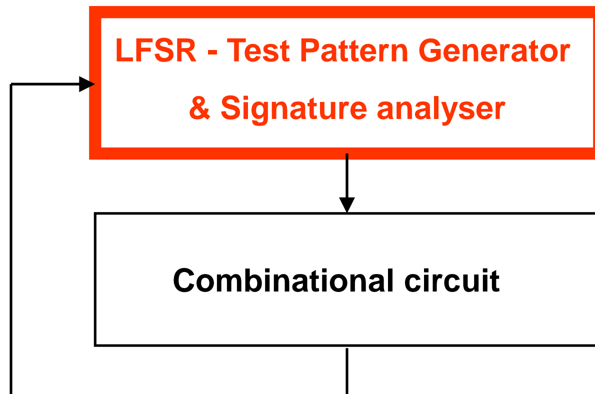
   Calculate the increase of the circuit size

   (in number of 2-input gates)

   due to adding of self-test circuitry

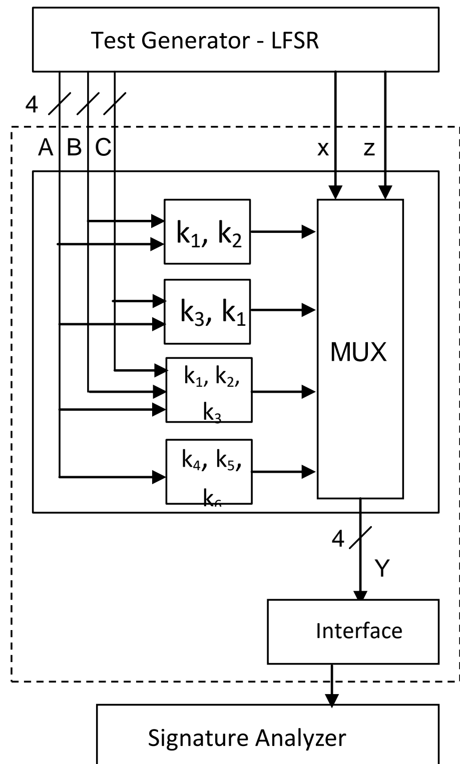
Course Work: Design of a Test Generator

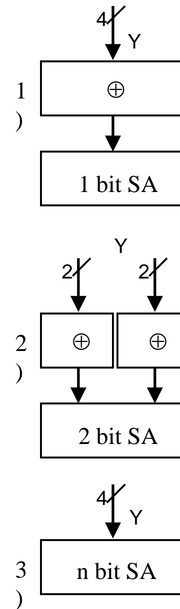
CSTP - Circular Self-Test Path:



8. Repeat the previous task for the case of using CSTP
   ("Circular Self Test Path")

Course Work: Design of a Response Analyzer





9. Carry out experiments with the test sets found in tasks 4 and 7

for 4 Signature Analyzers (SA):
1-bit, 2-bit, 4-bit, and 8-bit

Calculate the fault coverages for both tests

Draw the graphics *P = f(SA)*

P – is the fault coverage and
SA – is the number of bits in the Signature Analyzer

Draw 4 graphics *P = f(T)* for 4 SAs

T (test length) – changes from 0% to 100% of fault coverage

Explain the graphics (dependence on two factors: test quality *P = f(T)* , and response analysis quality *P = f(SA)*)

Course Work: Store-and-Generate BIST

11. Compare the results in tasks 4, 7, and 8. Which solution is the best and why?
12. Present the results of experiments